

Shark Bay Platform

PCB Version	-1
Project name	General-SFF
Project Code	91.3KZ01.001
PCB Number	12127
PCB Size	244mmX 200mm, t=1.6mm, 4-layers
PCB P/N	48.3KZ06.011
SCH Ver	A00

On Board Header and Jump setting

CONN	Default	DESCRIPTION
MECLR1	1-X	FOR AUD_LINK_SDO_R ENABLE AND FLASH
CMCLR1	1-3	Reset CMOS data (Debug Only)
PWCLR1	1-3	PASSWORD CLEAR
USBF3		2X10 pin USB3.0 header
USBF1		2X5 pin USB2.0 header
AUDF1		2X5 Front Panel Audio header
FNCPU1		1X4 pin CPU FAN
ATX1		2X12 ATX POWER CONN
XDPC1		60 pin XDP connector for CPU
LPC1		2X7 LPC debug port header (Debug Only)
LEDH1		2X6 Front Panel Header
USBF2		2X5 pin USB2.0 header
ATX12V		2X2 ATX12V POWER CONN

Board ID

[4..1]	Description
1110	

Major IC version/part number/vender

FUNCTION	Description	Version	WST P/N	Vendor
PCH		C1		INTEL
Realtek Lan	IC LAN RTL8151GD-CG QFN 32P(DELL)		71.08151.M06	REALTEK
SIO	IC SUPER IO IT8772E/EX LQFP 64P		71.08772.B0G	ITE
Audio Codec	IC AUDIO CODEC ALC3600-CG LQFP 48P		71.03600.00G	REALTEK

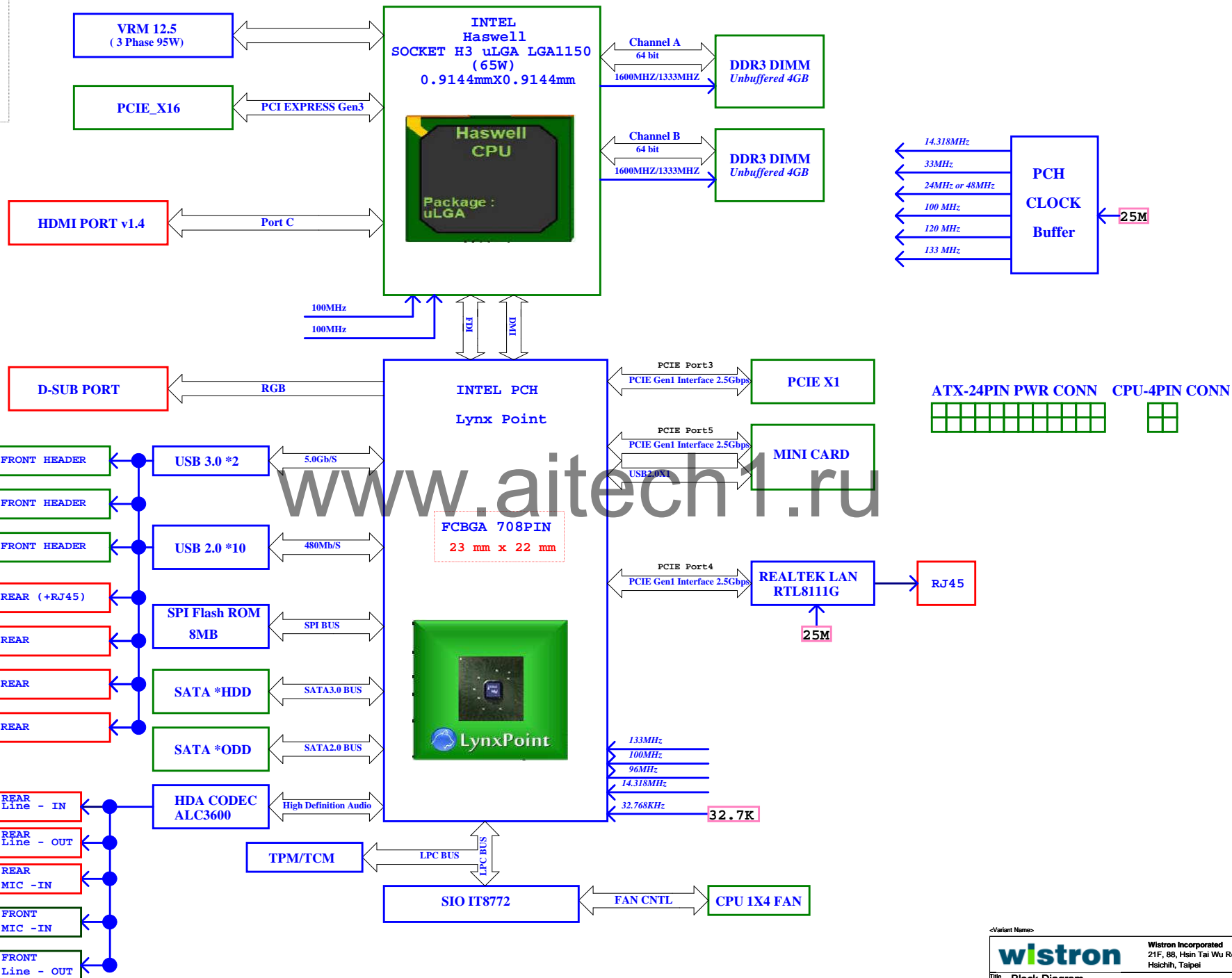
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15	DDR3 CHA DIMM 0	
16	TBD	
17	DDR3 CHB DIMM 0	
18	TBD	
19	Lynxpoint AUDIO/GPIO/SPI	
20	Lynxpoint_CLK	
21	Lynxpoint SATA/FAN/DP/VGA	
22	Lynxpoint_FDI/PCIE/DMI/USB	
23	Lynxpoint_GND/STRAPS	
24	Lynxpoint_POWER	
25	SATA Port	
26	PCIEX16 CONNECTOR	
27	VGA Port	
28	HDMI Port	
29	Display Port (TBD)	
30	FRONT USB3.0&2.0 HEADER	
31	USB+RJ45	
32	TBD	
33	REAR USB3.0	
34	USB2.0	
35	LAN RTL8151GD	
36	AUDIO CODEC ALC3600	
37	AUDIO CODEC JACKS	
38	TBD	
39	SIO ITE8772	
40	FAN CIRCUITS/HOLE	
41	TPM(NEW)	
42	PCIEX1 CONNECTOR	
43	MINI PCIE SLOT	
44	EMC(TBD)	
45	PWR/FNT PNL	
46	DUAL POWER	
47	DDR POWER	
48	SYSTEM POWER	
49	TBD	
50	CPU_VRD 12-5_1	
51	CPU_VRD 12-5_2	

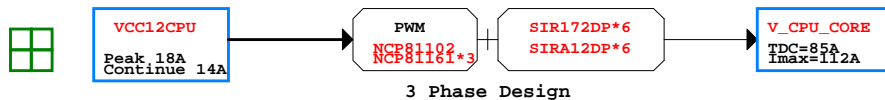
BOM Configuration
Unmount: (R)

PCB BOARD SIZE
200mmX 244mm
4 Layer

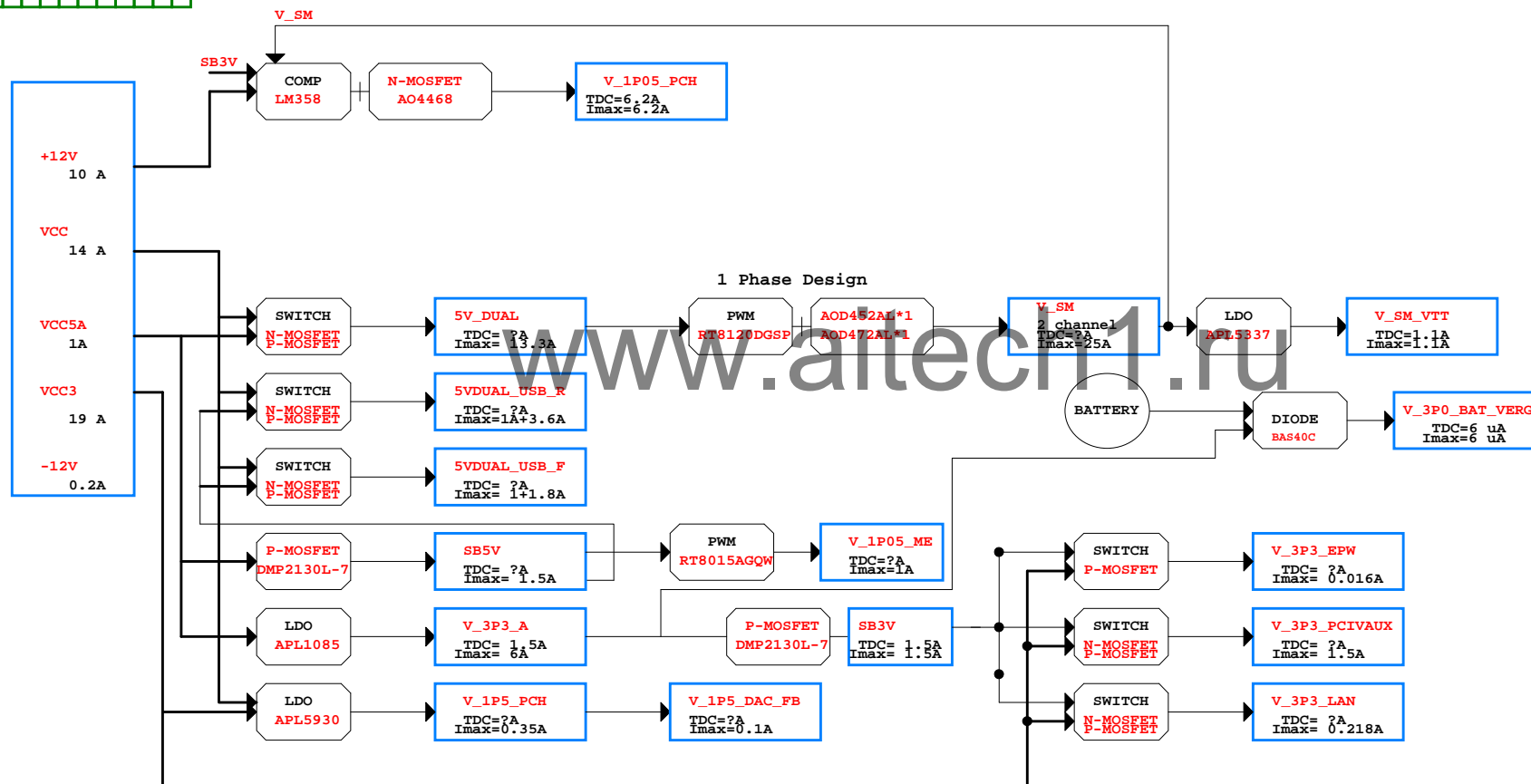
Internal Slot/Header
Front/Rear IO
Chipset



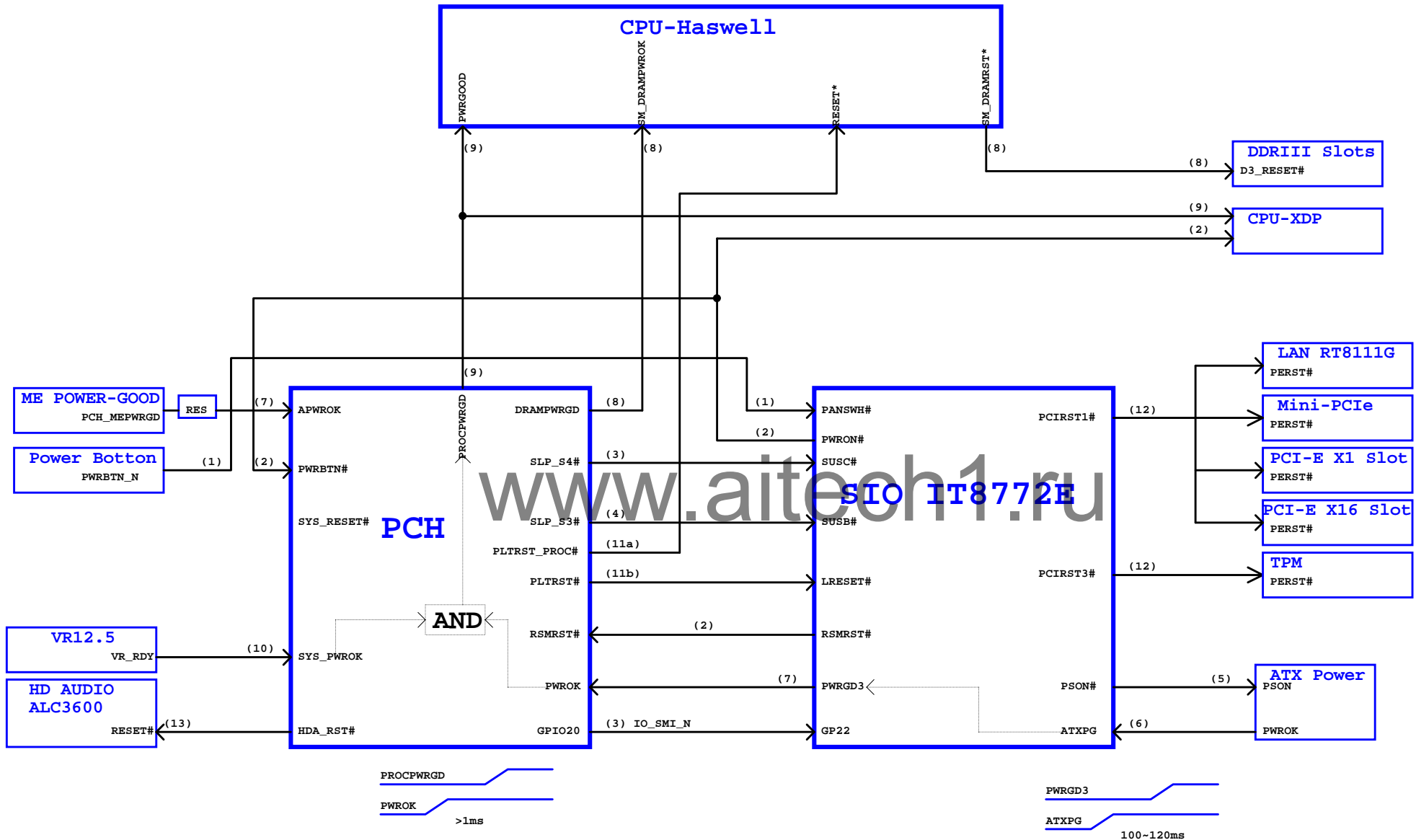
CPU 2X2 POWER CONN

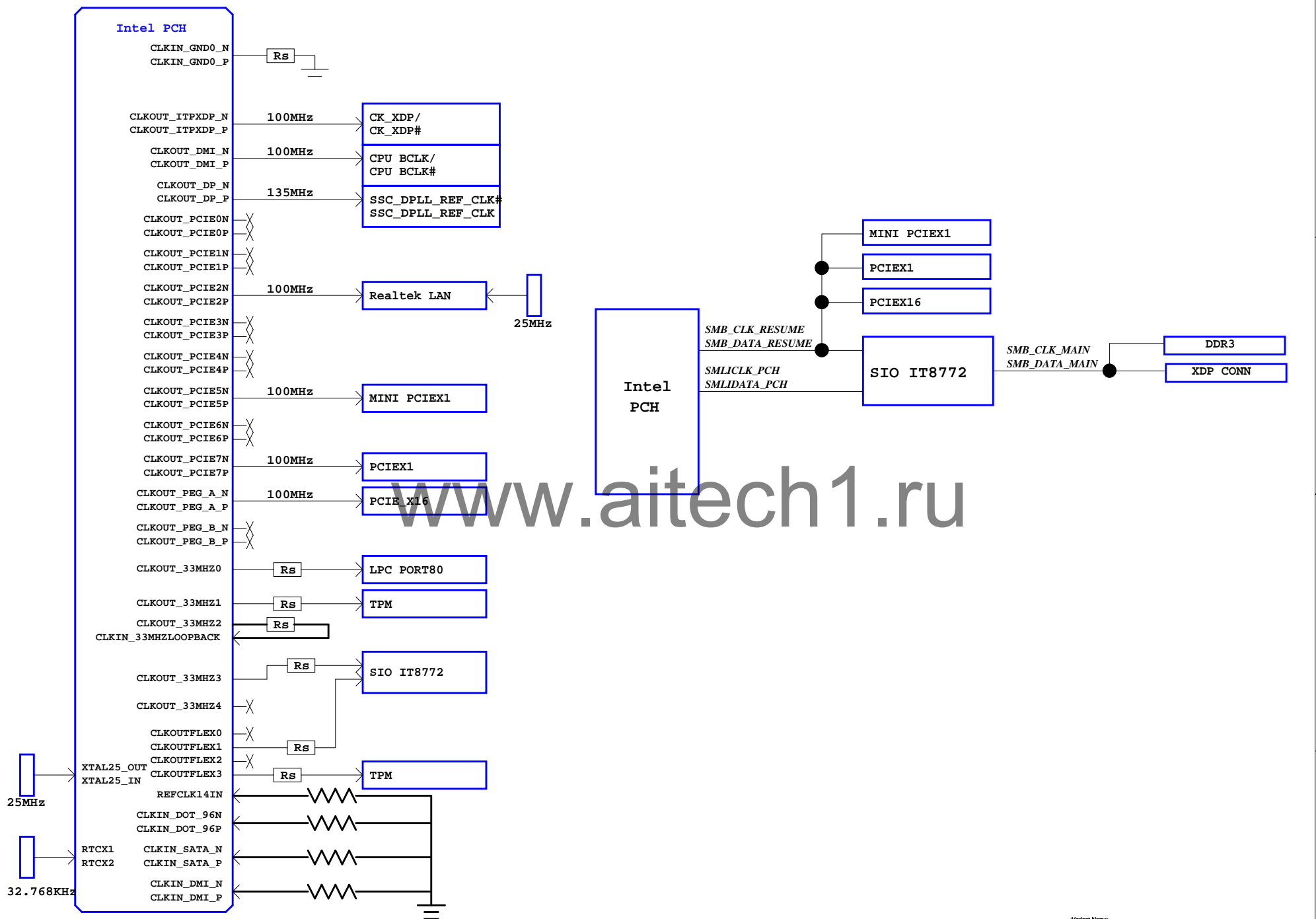


ATX 2X12 POWER CONN



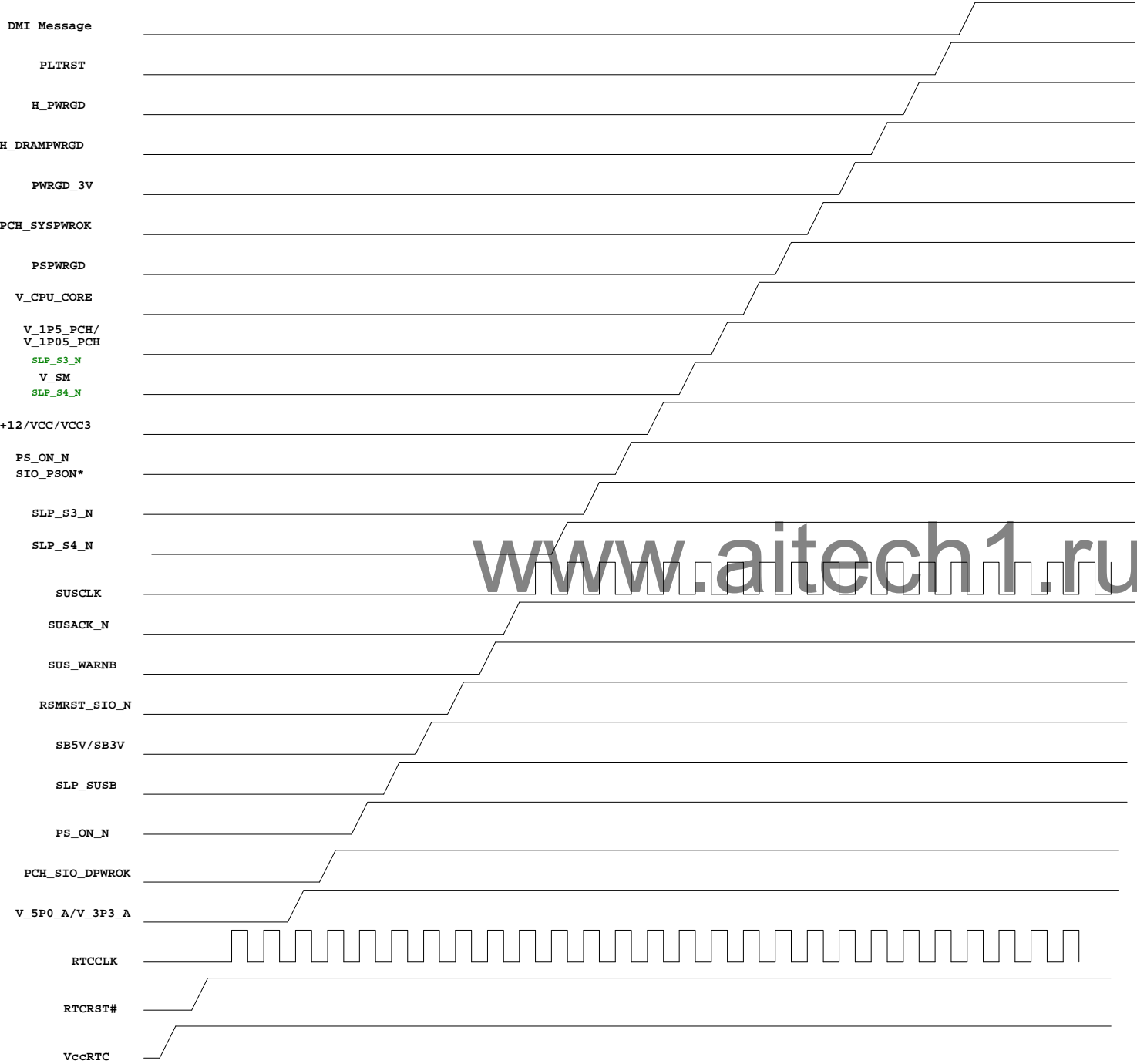
RESET / Power Good MAP



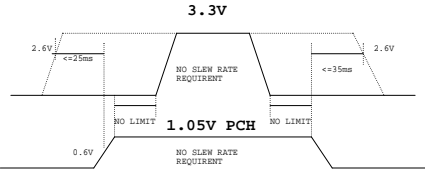


Note: is Reserve
Note: Rs is series resister

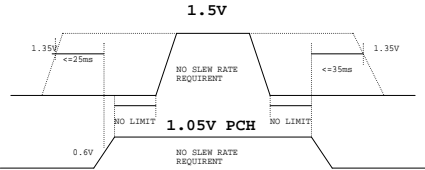
POWER ON SEQUENCE



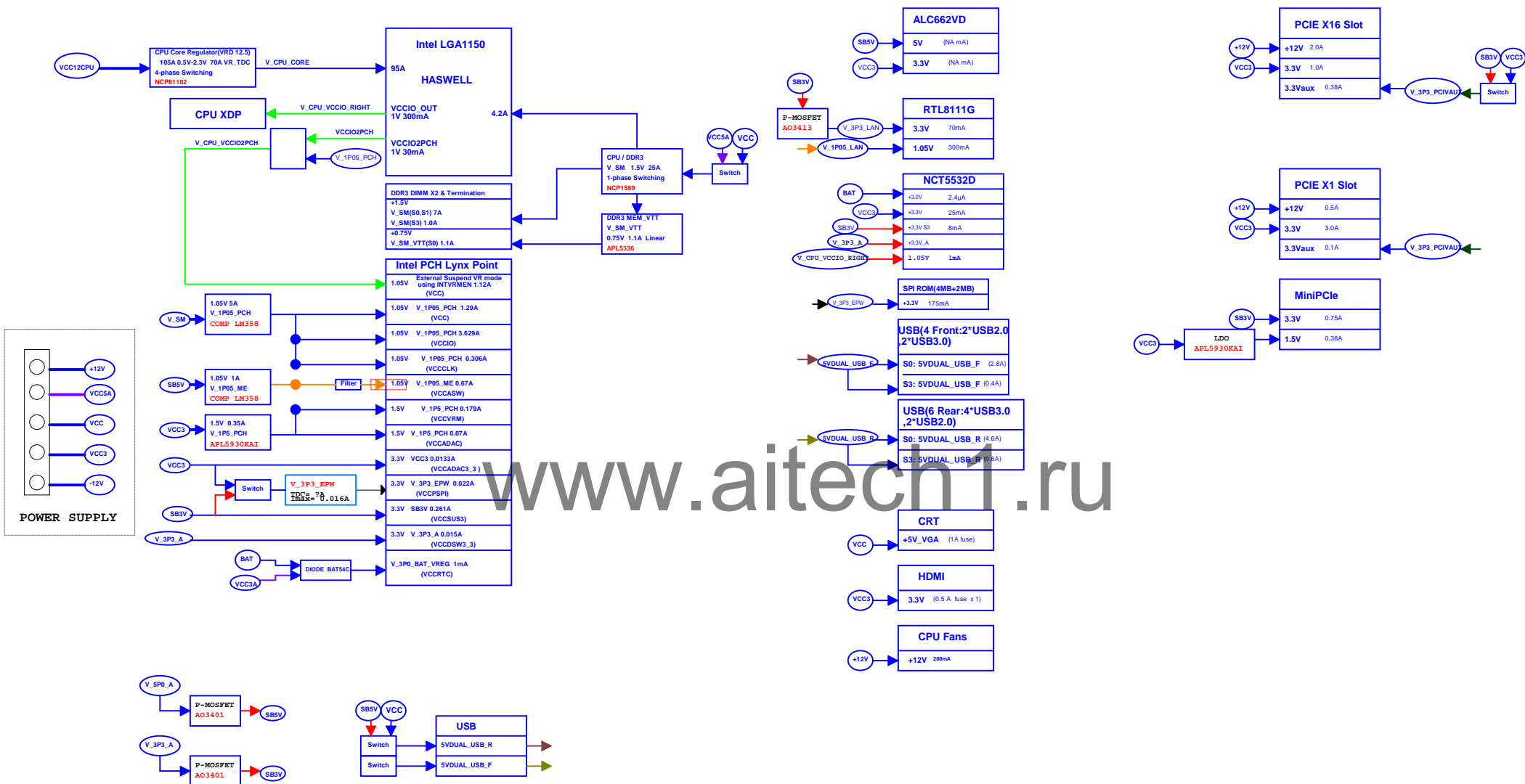
Sequencing Requirements between PCH VCC3_3 and VCC Core Rail



Sequencing Requirements between PCH VCC3_3 and VCC Core Rail




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TBD

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Title		
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TBD

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		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title TBD			
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CLOCK

20 CK_PE_100M_MCP_DN
20 CK_PE_100M_MCP_DP

CPU_VCORE

50 VCC_SENSE
50 VSS_SENSE
50 H_VIDSCK_VR
50 H_VIDSCK_VR
50 H_VIDALERT_N_VR

XDP

14 H_TDO
14 H_TDI
14 H_TMS
14 H_TRST_N
14 H_PROG_N
14 H_PREG_N

14 XDP_DRESET_N
14 HSW_XDP_MBP_0
14 HSW_XDP_MBP_1

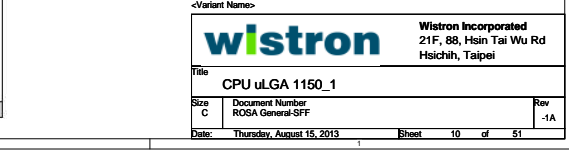
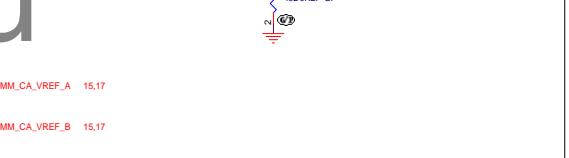
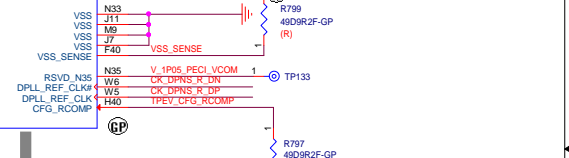
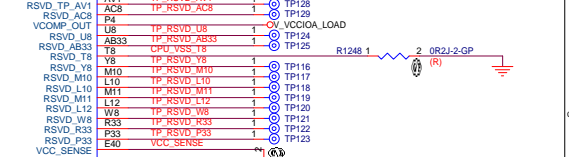
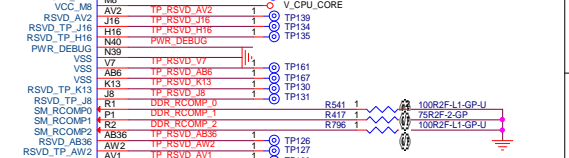
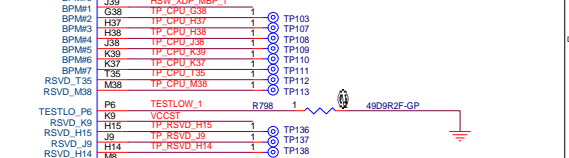
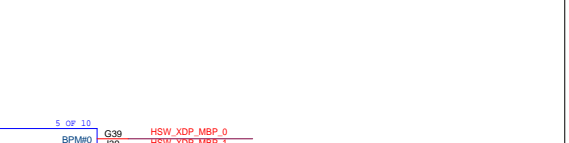
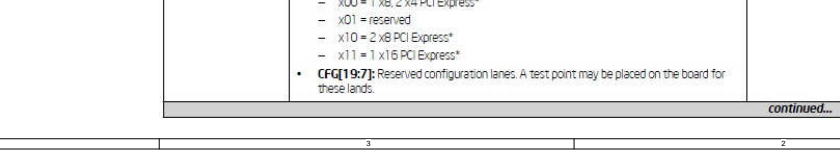
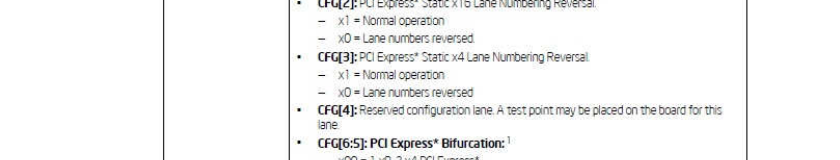
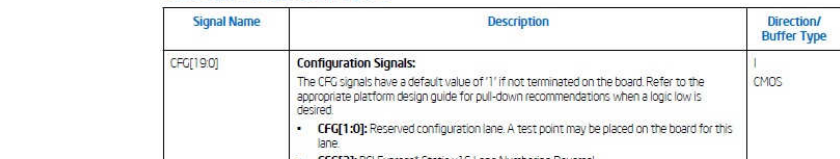
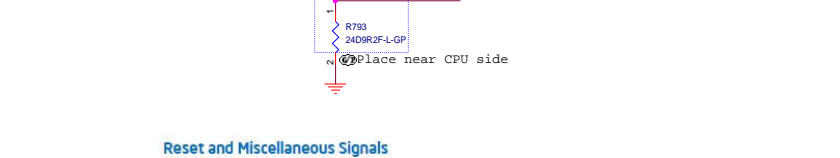
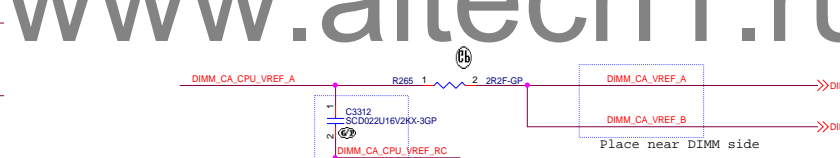
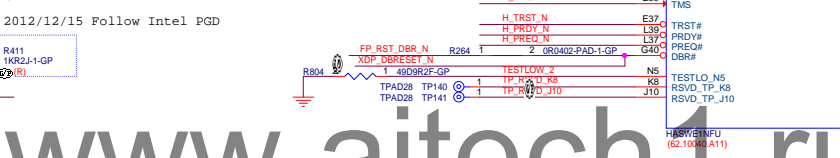
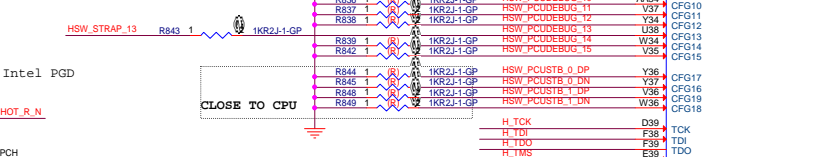
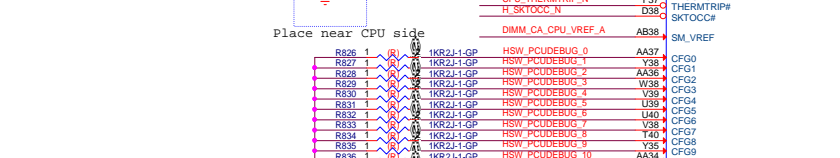
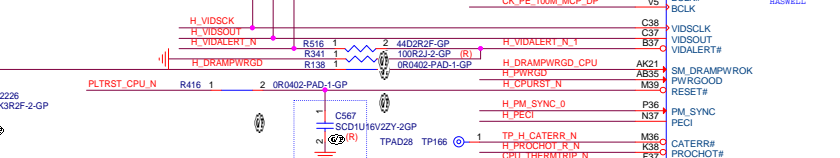
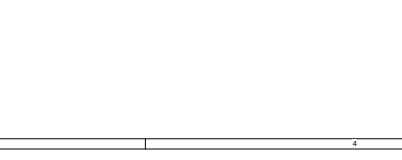
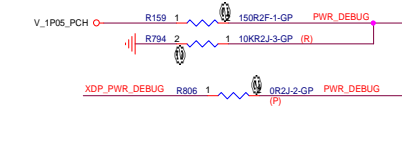
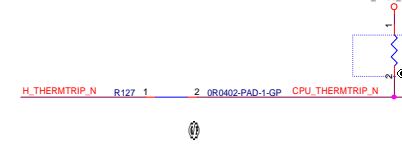
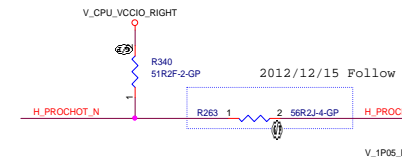
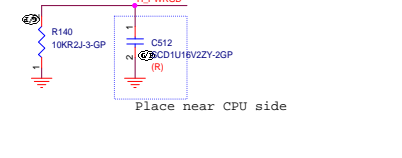
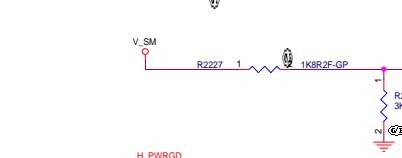
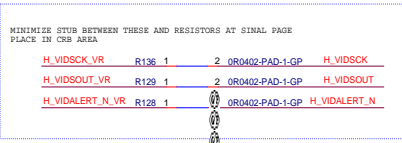
14 HSW_PCODEBUG_0
14 HSW_PCODEBUG_1
14 HSW_PCODEBUG_2
14 HSW_PCODEBUG_3
14 HSW_PCODEBUG_4
14 HSW_PCODEBUG_5
14 HSW_PCODEBUG_6
14 HSW_PCODEBUG_7
14 HSW_PCODEBUG_8
14 HSW_PCODEBUG_9
14 HSW_PCODEBUG_10
14 HSW_PCODEBUG_11
14 HSW_PCODEBUG_12
14 HSW_PCODEBUG_13
14 HSW_PCODEBUG_14
14 HSW_PCODEBUG_15

14 HSW_PCODEBUG_0_DP
14 HSW_PCODEBUG_0_DN
14 HSW_PCODEBUG_1_DP
14 HSW_PCODEBUG_1_DN
23 HSW_STRAP_13

OTHER

13_VCCST
14 XDP_PWR_DEBUG
14 HSW_PWR_DEBUG
19 FP_RST_DNR_N
19.50 H_SKTOCC_N
19.46 H_DRAMPWRGD
20 CK_DPMS_R_DP
20 CK_DPMS_R_DP
21 H_PM_SYNC_0
21.39 H_PECI

14.21 PLTRST_CPU_N
50 H_PROCHOT_N
21 H_THERMTRIP_N



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Reset and Miscellaneous Signals

Signal Name	Description	Direction/Buffer Type
CFG[19:0]	<p>Configuration Signals:</p> <p>The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> CFG[1:0]: Reserved configuration lane. A test point may be placed on the board for this lane. CFG[2]: PCI Express® Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> x1 = Normal operation x0 = Lane numbers reversed CFG[3]: PCI Express® Static x4 Lane Numbering Reversal. <ul style="list-style-type: none"> x1 = Normal operation x0 = Lane numbers reversed CFG[4]: Reserved configuration lane. A test point may be placed on the board for this lane. CFG[6:5]: PCI Express® Bifurcation:¹ <ul style="list-style-type: none"> x00 = 1 x8, 2 x4 PCI Express® x01 = reserved x10 = 2 x8 PCI Express® x11 = 1 x16 PCI Express® CFG[19:7]: Reserved configuration lanes. A test point may be placed on the board for these lands. 	CMOS

continued...

<Variant Name>

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Hsichih, Taipei

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PCIEX16

26 EXP_A_RX_DP0_15] <<<
26 EXP_A_TX_DN0_15] <<<
26 EXP_A_RX_DP0_15] <<<
26 EXP_A_TX_DN0_15] <<<

DMI

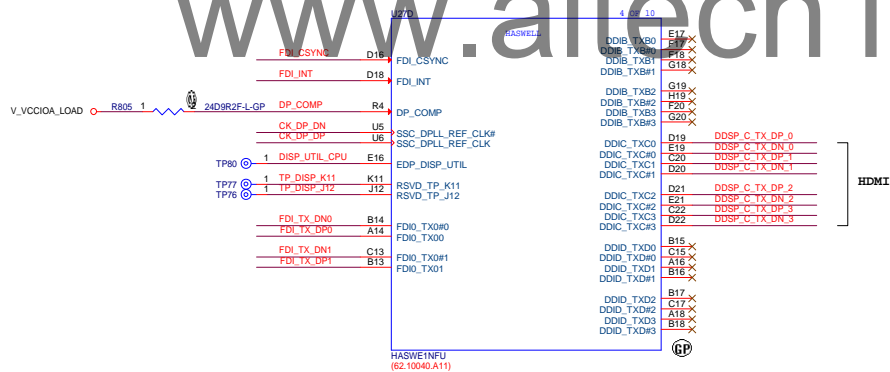
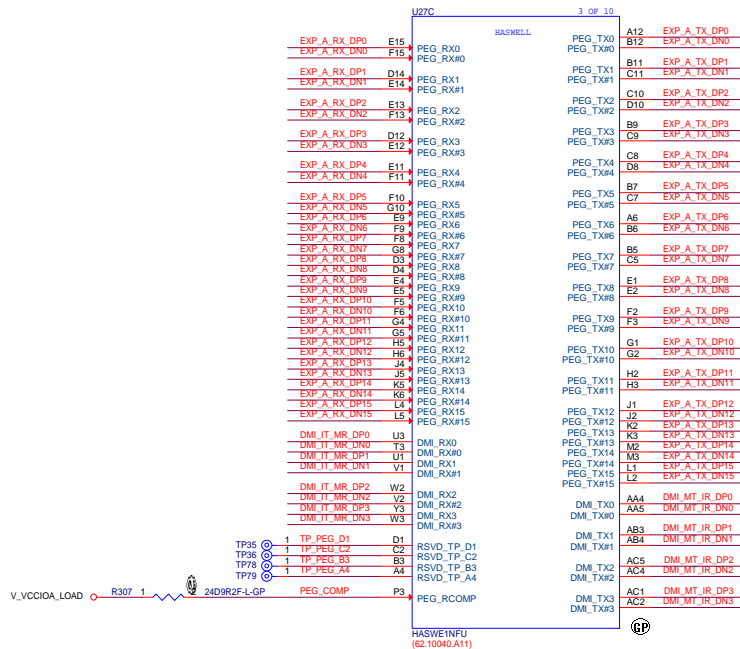
22 DMI.IT_MR_DP0_3] <<<
22 DMI.IT_MR_DN0_3] <<<
22 DMI.IT_MR_DP0_3] <<<
22 DMI.IT_MR_DN0_3] <<<

FDI

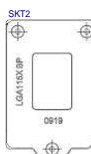
22 FDI_CS[SYNC] <<<
22 FDI_INT <<<
22 FDI_TX_DN0_1] <<<
22 FDI_TX_DP0_1] <<<
20 CK_DP_DP <<<
20 CK_DP_DN <<<

HDMI

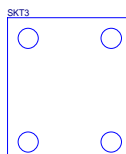
28 DDSP_C_TX_DP_0 <<<
28 DDSP_C_TX_DN_0 <<<
28 DDSP_C_TX_DP_1 <<<
28 DDSP_C_TX_DN_1 <<<
28 DDSP_C_TX_DP_2 <<<
28 DDSP_C_TX_DN_2 <<<
28 DDSP_C_TX_DP_3 <<<
28 DDSP_C_TX_DN_3 <<<



Load Plate
(22.78003.021)



Back Plate
(22.78006.031)



BACK PLATE
(60.3EQ19.001)



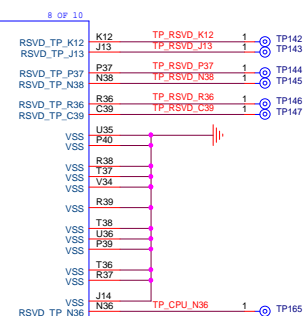
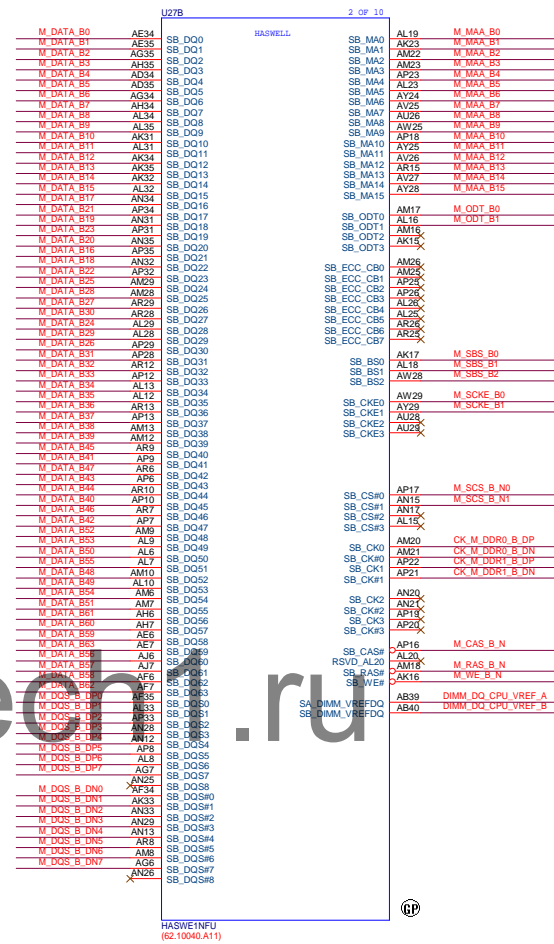
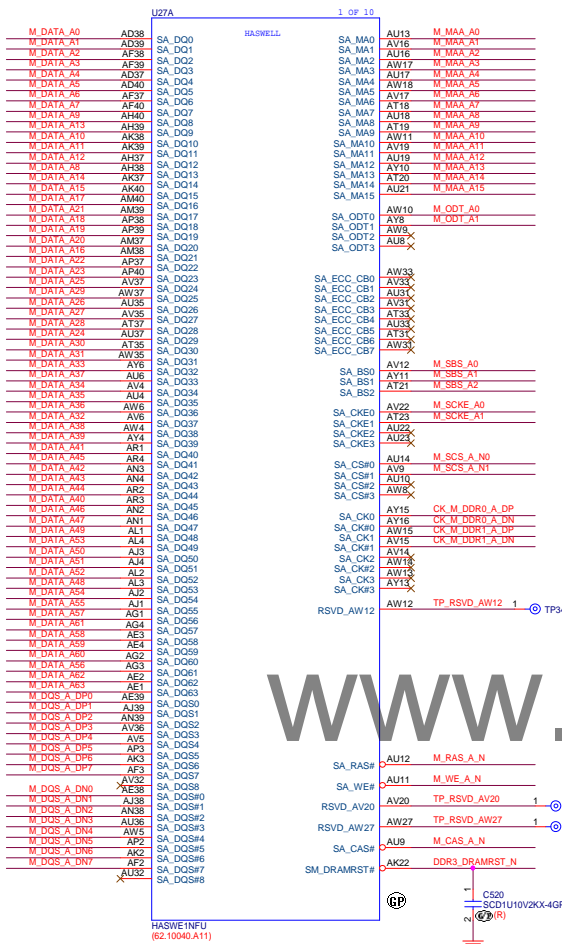
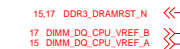
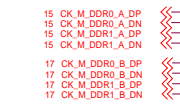
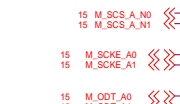
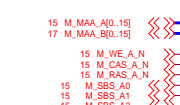
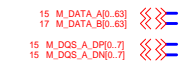
ILMCOVER
(42.3EQ28.002)

<Variant Name>

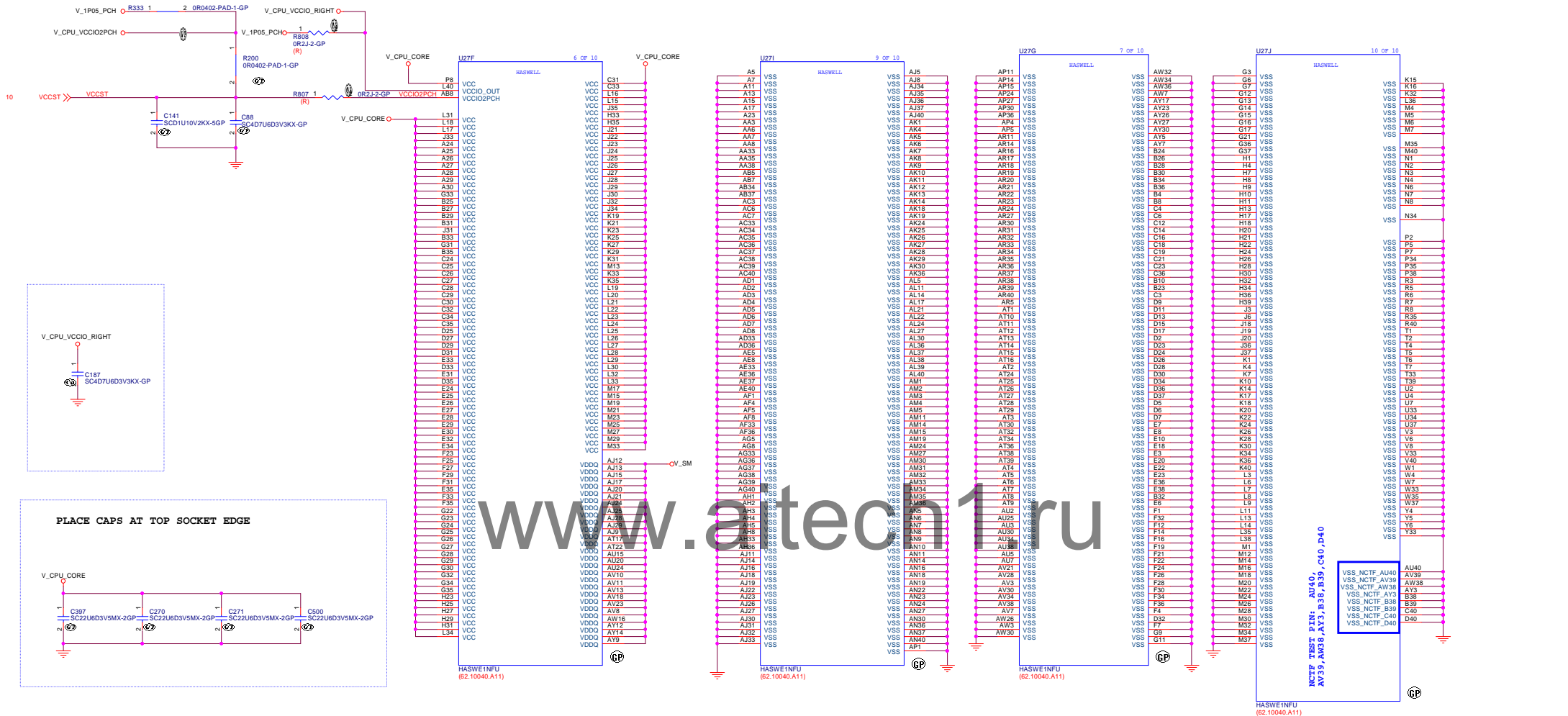
wlstron

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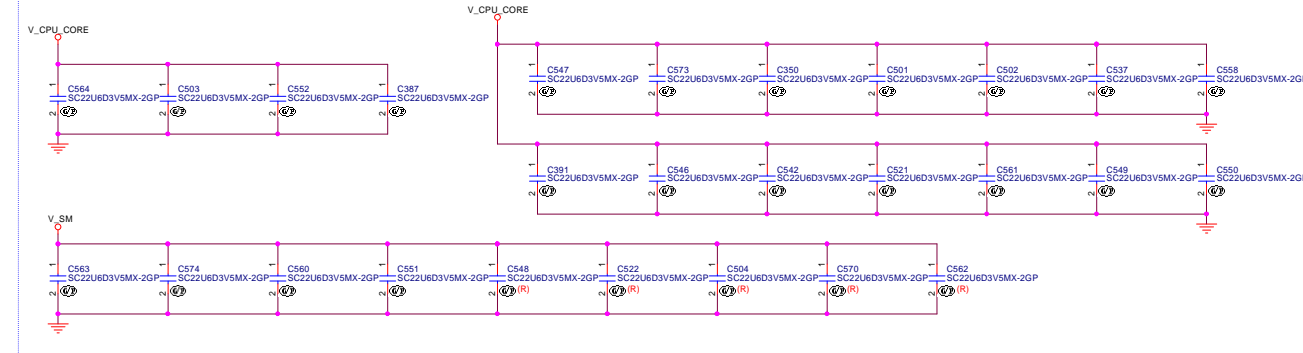
File CPU uLGA 1150_2		
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Put R333 near PCH side for V_CPU_VCCIO2PCH is for PCH power



PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY



DEFENSIVE DESIGN PWR_DEBUG

2012/12/04 Ryan removed,

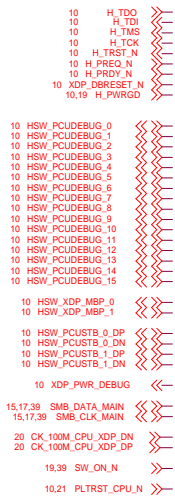
CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	22
V_SM	22uf 0805	4+5(R)

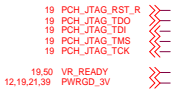
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File	CPU uLGA 1150_4		
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XDP for CPU



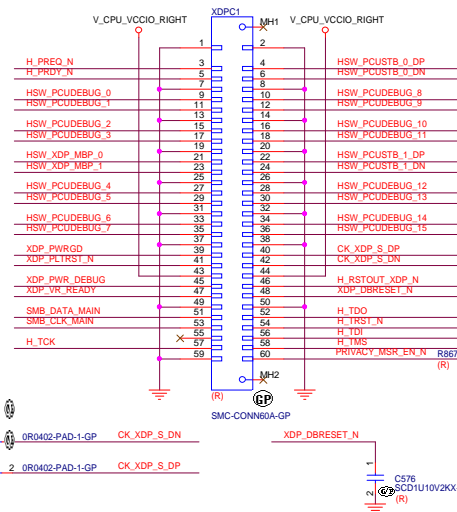
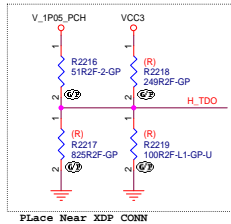
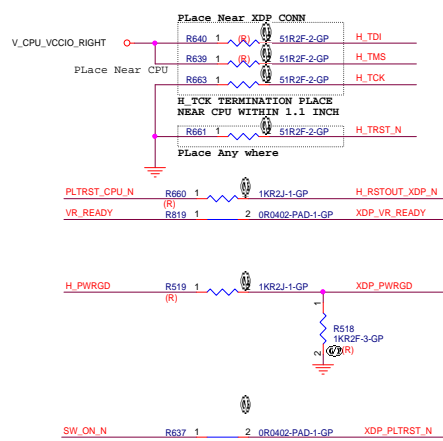
XDP for PCH



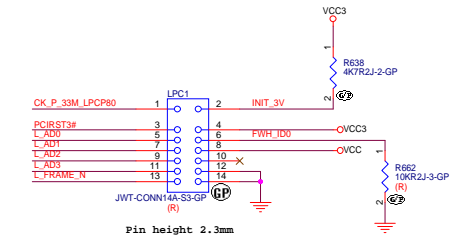
LPC DEBUG PORT



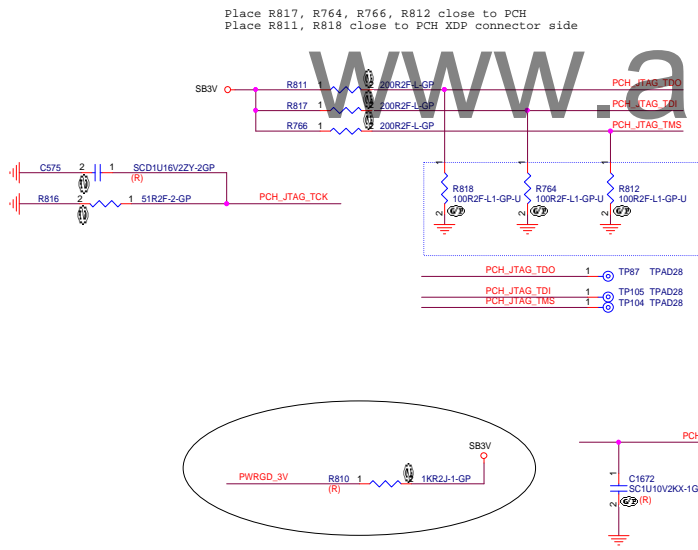
XDP for CPU



LPC DEBUG PORT



XDP for PCH



2012/12/15 delete reserve R815

<Variant Name>

wlstron Wistron Incorporated
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Hsichih, Taipei

File		
XDP/80 PORT HEADER/APS		
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DDR DATA

DDR CMD/ADD

12	M_MAA_A[0..15]	←
12	M_WE_A_N	←
12	M_CAS_A_N	←
12	M_RAS_A_N	←
12	M_SBS_A0	←
12	M_SBS_A1	←
12	M_SBS_A2	←

DDR CTRL

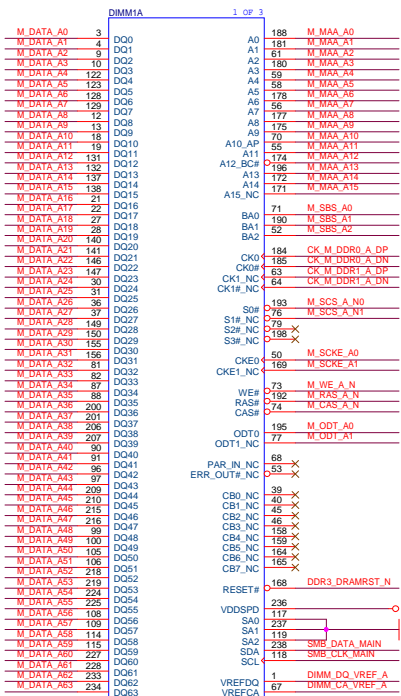
12	M_SCS_A_N0	↔
12	M_SCS_A_N1	↔
12	M_SCKE_A0	↔
12	M_SCKE_A1	↔
12	M_ODT_A0	↔
12	M_ODT_A1	↔

DDR CLOCK

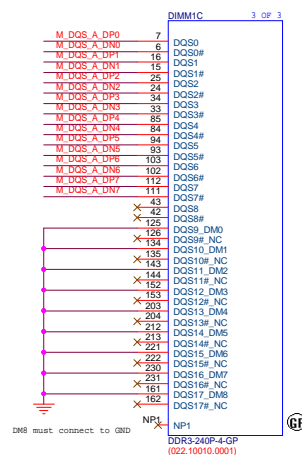
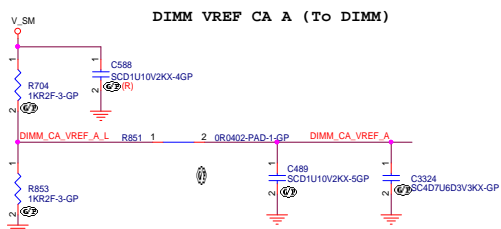
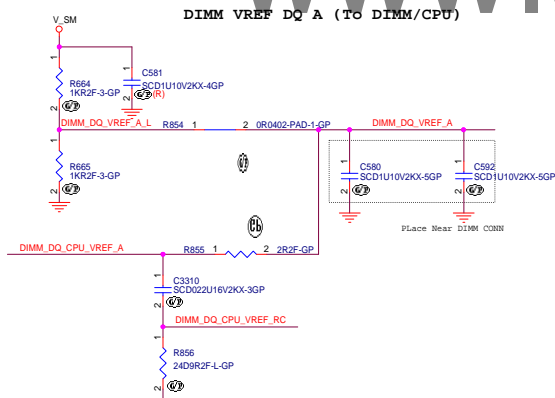
12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

DDR OTHERS

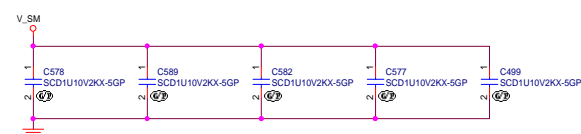
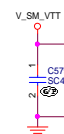
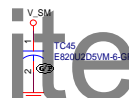
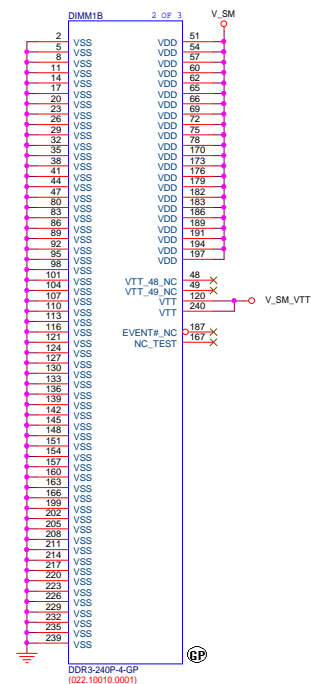
14,17,39	SMB_DATA_MAIN	《	》
14,17,39	SMB_CLK_MAIN	《	》
12,17	DDR3_DRAMRST_N	《	》
12	DIMM_DQ_CPU_VREF_A	《	》
10,17	DIMM_CA_VREF_A	《	》



Trace: 12/12 mils



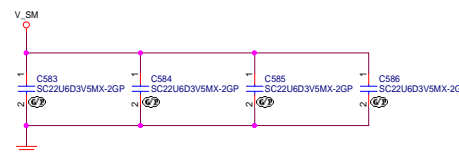
SMB ADDRESS: 000
SPD R/W: 0*A1, 0*A0



Place Near Power Pin

Net	CAP	Qty
V_SM	0.1uf 0402 X5R	5+4
V_SM_VTT	4.7uf 0603 X5R	1
V SM VTT	0.1uf 0402 X5R	1


CAPS FOR DIMM



TBD

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<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title TBD		
Size A	Document Number ROSA General-SFF	Rev -1A
Date:	Thursday, August 15, 2013	Sheet 16 of 51

TBD

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<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title TBD		
Size A	Document Number ROSA General-SFF	Rev -1A
Date:	Thursday, August 15, 2013	Sheet 18 of 51

CPU CLOCK

10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP

PCI CLOCK

39 CK_P_33M_TPM
14 CK_P_33M_LPCP80
22 CK_PCH_33M_FB
30 CK_P_33M_SIO

PCIE CLOCK

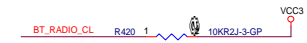
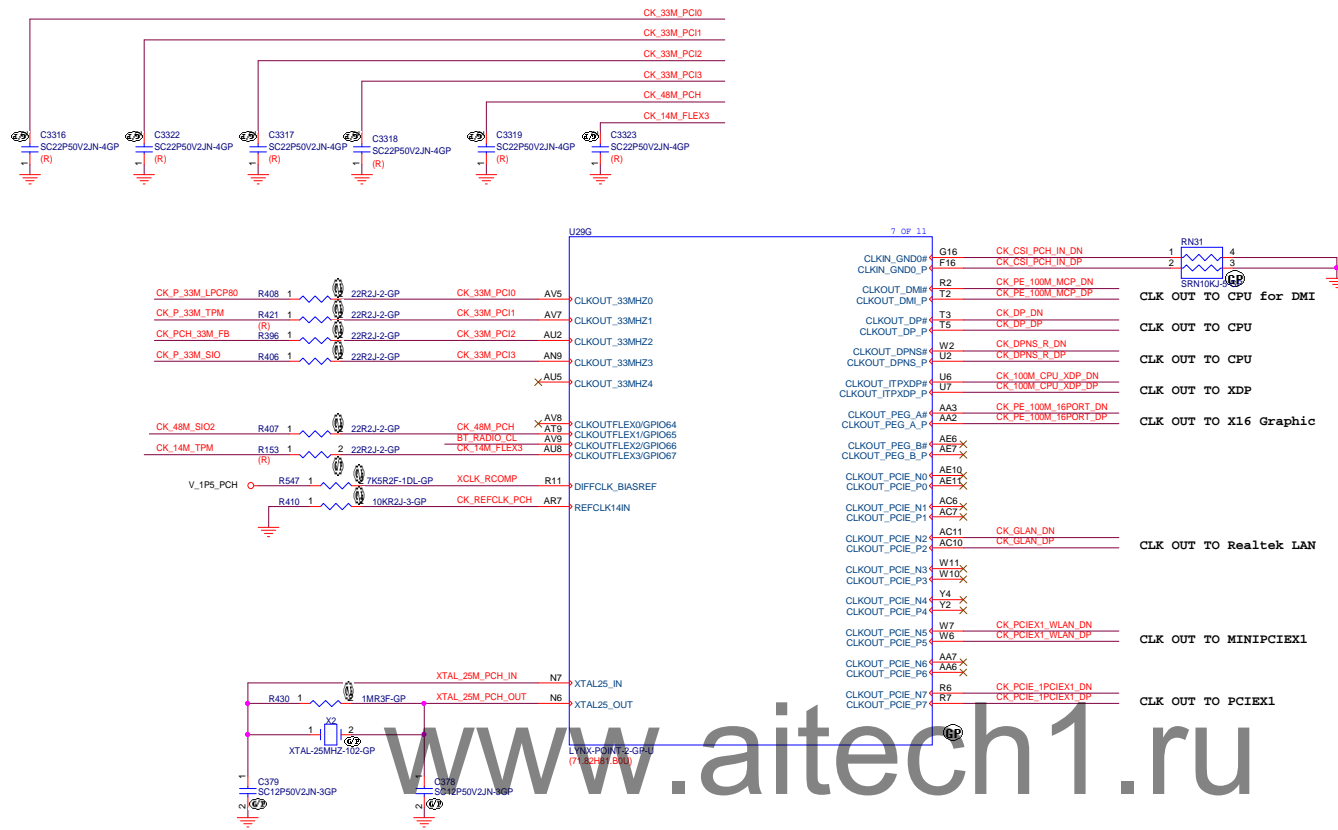
10 CK_DPNS_R_DN
10 CK_DPNS_R_DP
11 CK_DP_DN
11 CK_DP_DP
14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP
26 CK_PE_100M_16PORT_DN
26 CK_PE_100M_16PORT_DP
35 CK_GLAN_DN
35 CK_GLAN_DP
43 CK_PCIE1_WLAN_DN
43 CK_PCIE1_WLAN_DP
42 CK_PCIE1_PCIE1X1_DN
42 CK_PCIE1_PCIE1X1_DP

14M and 48M CLOCK

39 CK_48M_SIO2
39 CK_14M_TPM
39 CK_14M_TPM

GPIO

43 BT_RADIO_CL



7 OF 11

G16	CK_CSI_PCH_IN_DN	1	4
F16	CK_CSI_PCH_IN_DP	2	3
R2	CK_PE_100M_MCP_DN		
T2	CK_PE_100M_MCP_DP		
T3	CK_DP_DN		
T5	CK_DP_DP		
W2	CK_DPNS_R_DN		
U2	CK_DPNS_R_DP		
U6	CK_100M_CPU_XDP_DN		
U7	CK_100M_CPU_XDP_DP		
AA3	CK_PE_100M_16PORT_DN		
AA2	CK_PE_100M_16PORT_DP		
AE6	CK_GLAN_DN		
AE7	CK_GLAN_DP		
AE10	CK_PCIE1_WLAN_DN		
AE11	CK_PCIE1_WLAN_DP		
AC11	CK_PCIE1_PCIE1X1_DN		
AC10	CK_PCIE1_PCIE1X1_DP		
W11	CK_PCIE1_PCIE1X1_DN		
W10	CK_PCIE1_PCIE1X1_DP		
Y4	CK_PCIE1_PCIE1X1_DN		
Y2	CK_PCIE1_PCIE1X1_DP		
W7	CK_PCIE1_PCIE1X1_DN		
W6	CK_PCIE1_PCIE1X1_DP		
AA7	CK_PCIE1_PCIE1X1_DN		
AA6	CK_PCIE1_PCIE1X1_DP		
R6	CK_PCIE1_PCIE1X1_DN		
R7	CK_PCIE1_PCIE1X1_DP		

CLK OUT TO CPU for DMI
CLK OUT TO CPU
CLK OUT TO CPU
CLK OUT TO XDP
CLK OUT TO X16 Graphic
CLK OUT to Realtek LAN
CLK OUT TO MINIPCIEX1
CLK OUT TO PCIEX1

<Variant Name>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title Lynxpoint_CLK			
Size C	Document Number ROSA General-SFF		Rev -1A
Date:	Thursday, August 15, 2013	Sheet	20 of 51

25 SATAHDR_RX_DN0

25 SATAHDR_RX_DP0

25 SATAHDR_TX_DN0

25 SATAHDR_TX_DP0

25 SATAHDR_RX_DN1

25 SATAHDR_RX_DP1

25 SATAHDR_TX_DN1

25 SATAHDR_TX_DP1

39,45 PCH_SATA_LED_N <<-

23 SATA1GP >>—
23 SATA2GP >>—
23 SATA3GP >>—

```

10 H_PM_SYNC_0 <<
10,39 H_PCE1 <<
10 H_THERMTRIP_N <<
12,14,19,39 PWRGD_3V <<
36 FP_AUD_DETECT <<
39 A20GATE <<
39 KBST_N <<
39 SER_IRQ <<
10,14 PLTRST_CPU_N <<
26 PCIE16_PRSTN2_N <<
45 CHASSIS_ID_1 <<
45 CHASSIS_ID_0 <<
22 BOARD_ID_0 <<
42 PCIE1_PRSTN2_N <<

```

```


28 DDPC_CTRL_CLK  <= <<<>>>
28 DDPC_CTRL_DATA  <= <<<>>>

```

```

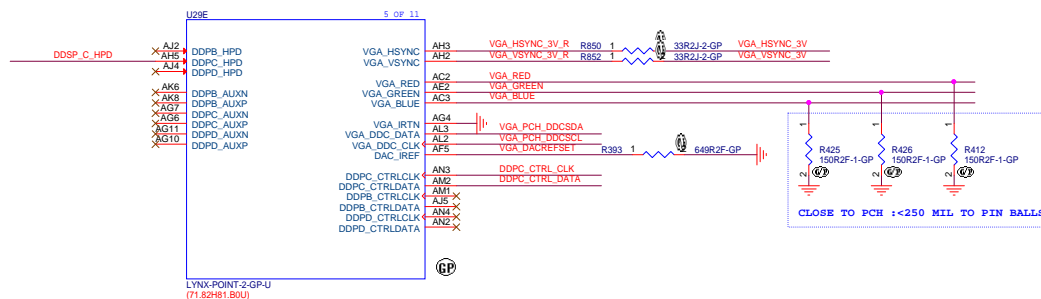
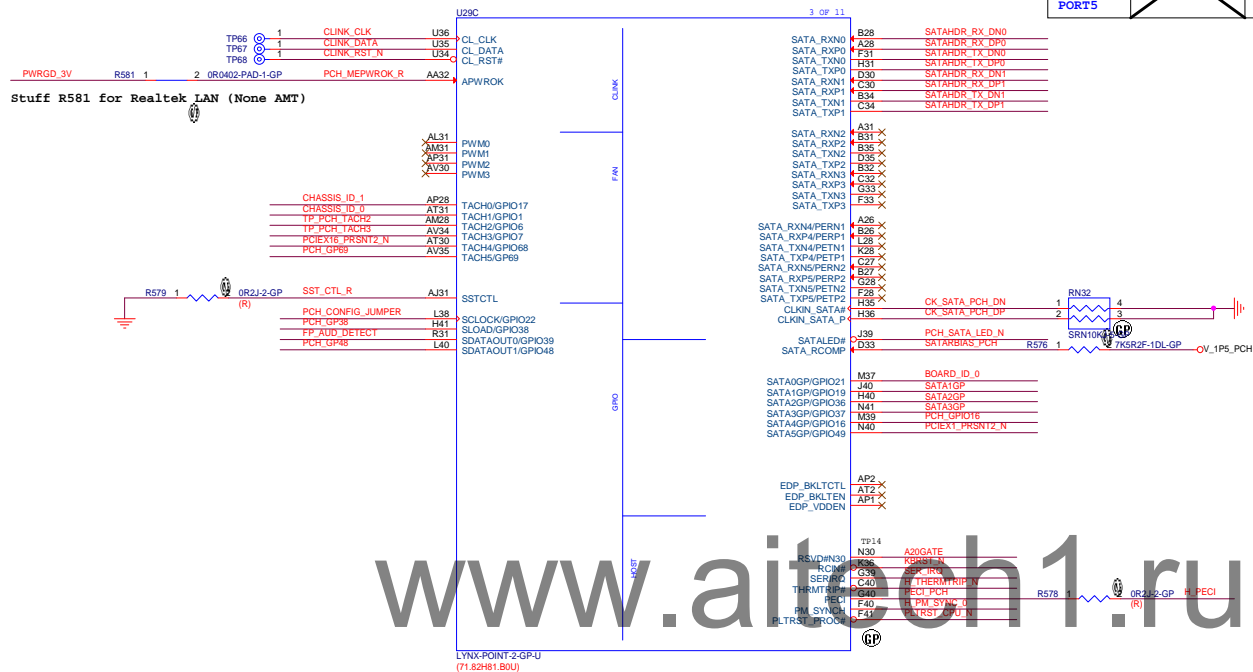
27 VGA_HSYNC_3V
27 VGA_VSYNC_3V
27 VGA_RED
27 VGA_GREEN
27 VGA_BLUE
27 VGA_PCH_DDCSDA
27 VGA_PCH_DDCSCL

```

SATA Port (H81)		
	SATA 3.0 PORT	SATA 2.0 Port
PORT0	Support	Support
PORT1	Support	Support
PORT2		Disabled
PORT3		Disabled
PORT4		Support
PORT5		Support

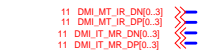
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GPIO49 CAN BE USE AS PCIE/MSATA MUX SELECT IN LPT

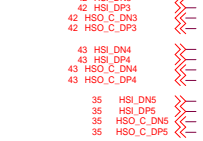


CLOSE TO PCH :<250 MIL TO PIN BALLS

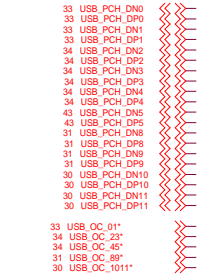
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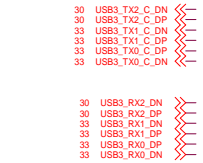
PCIE



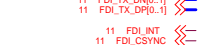
USB2.0



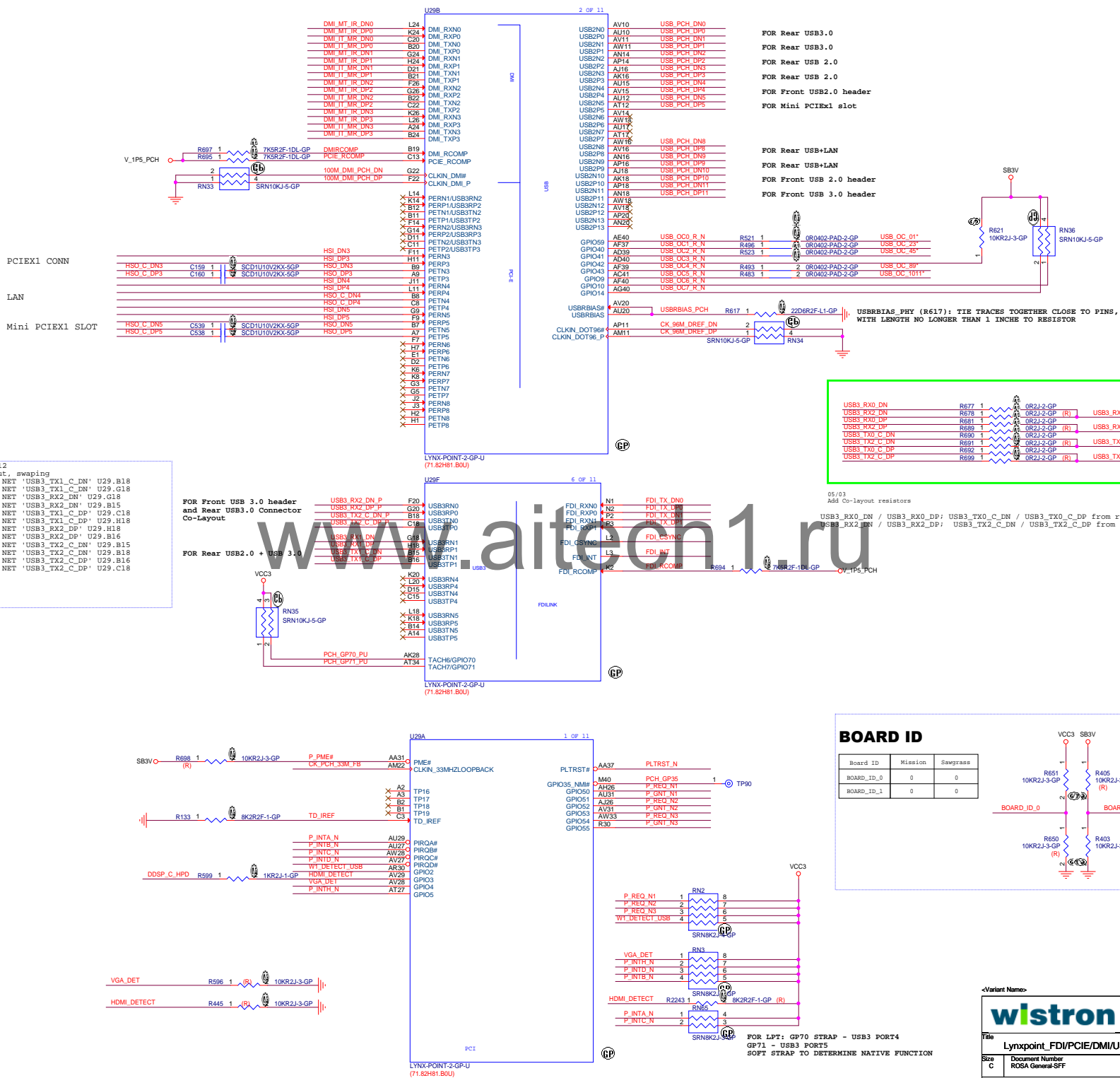
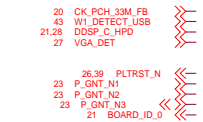
USB3.0



FDI

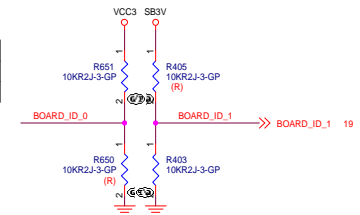


OTHERS



BOARD ID

Board ID	Mission	Sawgrass
BOARD_ID_0	0	0
BOARD_ID_1	0	0



<Variant Name:

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

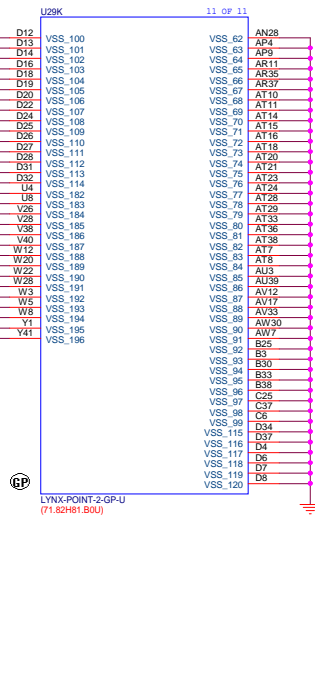
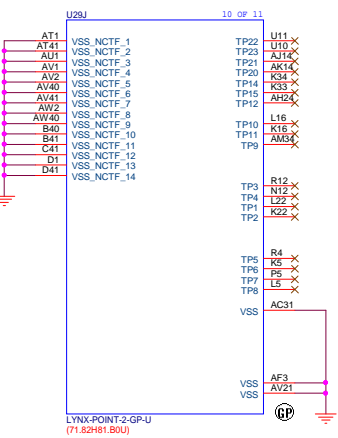
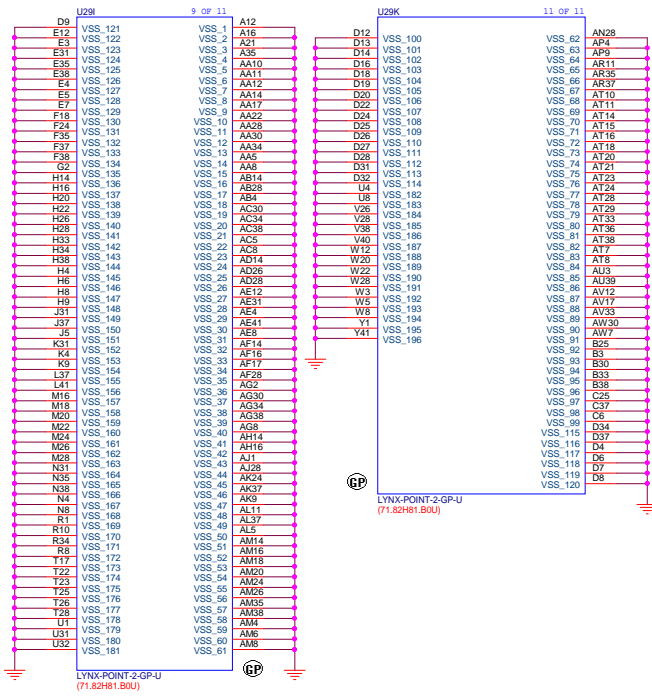
Title	Lynxpoint_FDI/PCIE/DMI/USB
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Date:	Thursday, August 15, 2013	Sheet 22 of 51

FOR LPT: GP70 STRAP - USB3 PORT4
GP71 - USB3 PORT5
SOFT STRAP TO DETERMINE NATIVE FUNCTION

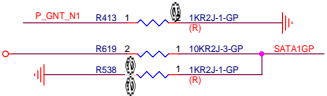
STRAP

- 21 SATA1GP
- 21 SATA2GP
- 21 SATA3GP
- 22 P_GNT_N1
- 10 HSW_STRAP_13
- 19 IGC_EN_N
- 19 AUD_LINK_SDO_R
- 19 SUSCLK
- 19 SPKR
- 22 P_GNT_N2
- 22 P_GNT_N3
- 19 PCH_INTVRMEN
- 19 DSWVRMEN
- 19 PCH_GP15

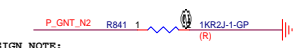


BOOT SELECT STRAPS

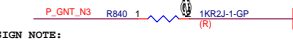
BOOT DEVICE	GNT1/ GPIO51	SATA1GP /GPIO19
LPC	0	0
SPI	1	1



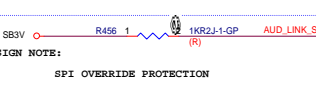
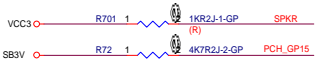
DESIGN NOTE:
WEAK INTERNAL PULLUPS ON GP51. DEFAULT SPI BOOT DEVICE.



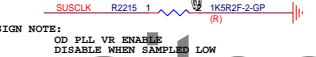
DESIGN NOTE:
FULL VOLTAGE MODE WHEN SAMPLED LOW
DMI AC COUPLING



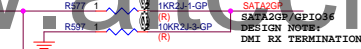
DESIGN NOTE:
A16 SWAP OVERRIDE OVERRIDE IF SAMPLED LOW



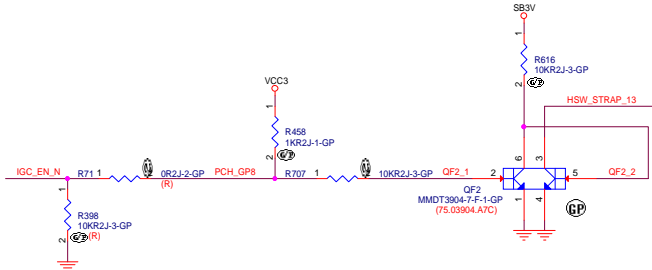
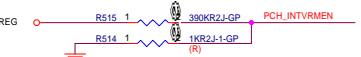
DESIGN NOTE:
SPI OVERRIDE PROTECTION



DESIGN NOTE:
OD PLL VR ENABLE
DISABLE WHEN SAMPLED LOW



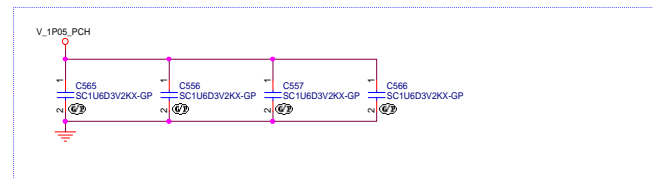
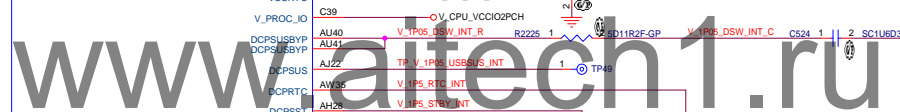
DESIGN NOTE:
LOW:TLS CIPHER SUITE WITH NO CONFIDENTIALITY.
HIGH:TLS CIPHER SUITE WITH CONFIDENTIALITY.



PCH Functional Straps

PCH EDS,Page88,Table 2-27

SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
INIT3_3VB	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low
P_GNT_N3	Top-Block Swap Override The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
PCH_INTVRMEN	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high
P_GNT_N1	Boot BIOS Destination Selection Signal has weak internal pull-ups.
SATA1GP (GPIO19)	Boot BIOS Destination Selection Signal has weak internal pull-ups.
P_GNT_N2	The signal has a weak internal pull-up.
AUD_LINK_SDO_R	Flash Descriptor Security Override Strap .
AUD_LINK_SYNC-R	The signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
PCH_GP28_PU (GPIO28) USB_CH_M2	The signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
DF_TVS	DMI and FDI Tx/Rx Termination Voltage The signal has a weak internal pull-down.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
CDC_DWN_DISABLE (SATA2GP/GPIO36)	DMI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
PCH_GP37 (SATA3GP/GPIO37)	FDI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal pull-down
TLS_EN (GPIO15)	The signal has a weak internal pull-down. Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality A strong pull up may be needed for GPIO functionality



21 SATAHDR_RX_DP0

21 SATAHDR_RX_DN0

21 SATAHDR_TX_DN0

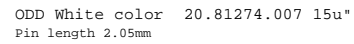
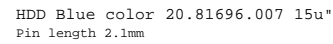
21 SATAHDR_TX_DP0

21 SATAHDR_RX_DP1

21 SATAHDR_RX_DN1

21 SATAHDR_TX_DN1

21 SATAHDR_TX_DP1



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PCIE16

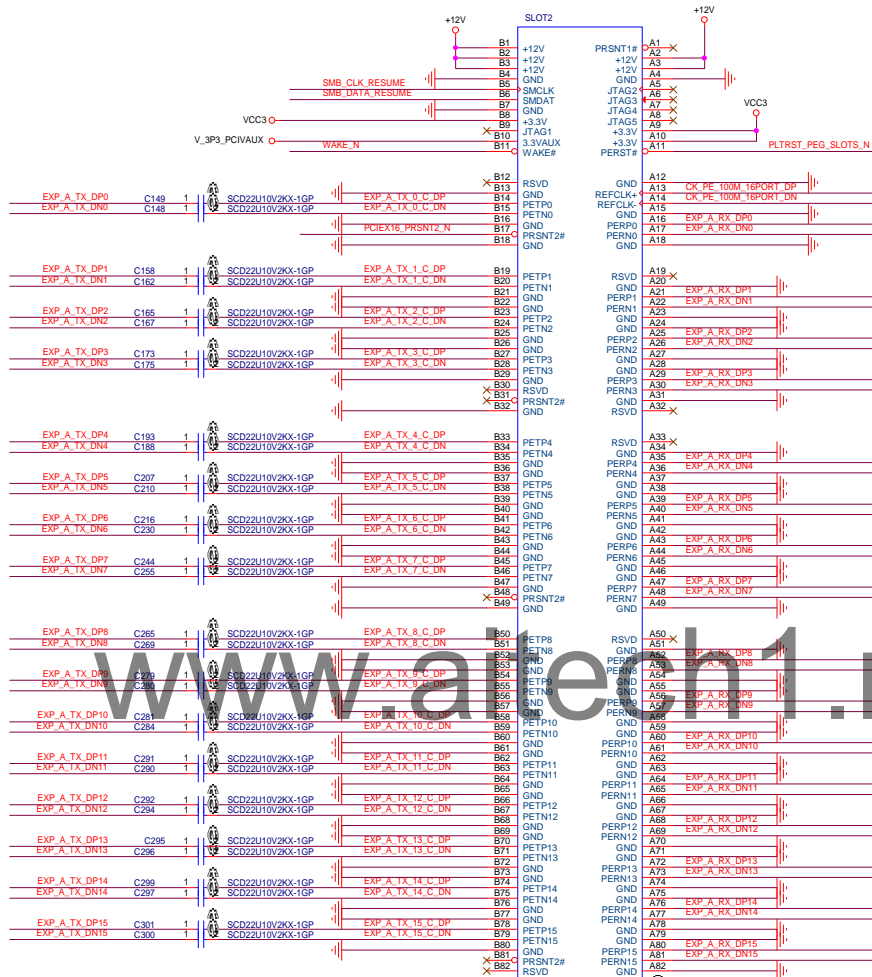
11 EXP_A_RX_DN[0..15]
11 EXP_A_RX_DP[0..15]
11 EXP_A_TX_DP[0..15]
11 EXP_A_TX_DN[0..15]
20 CK_PE_100M_16PORT_DP
20 CK_PE_100M_16PORT_DN

OTHERS

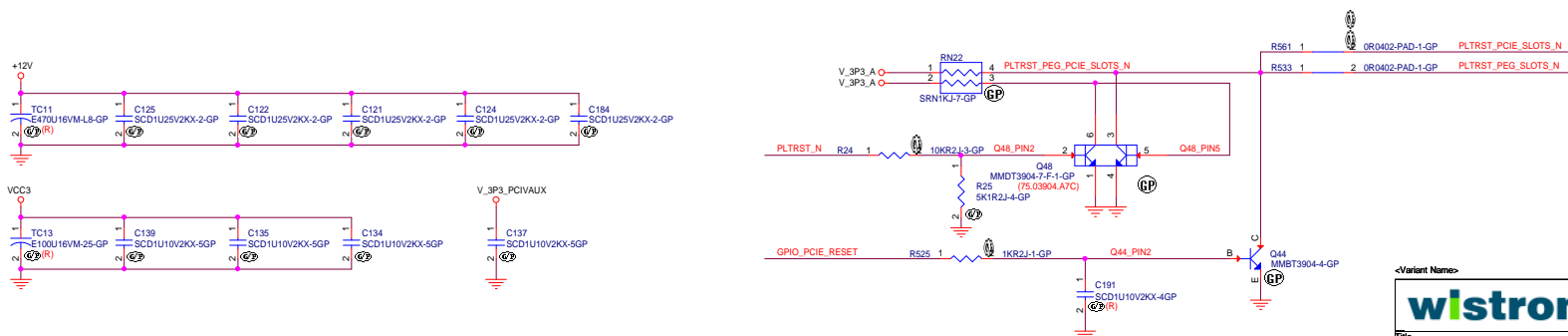
19,39,42,43 SMB_CLK_RESUME
19,39,42,43 SMB_DATA_RESUME
19,35,42,43 WAKE_N
21 PCIE16_PRSNT2_N
19 GPIO_PCIE_RESET
22,39 PLTRST_N
42,43 PLTRST_PCIE_SLOTS_N

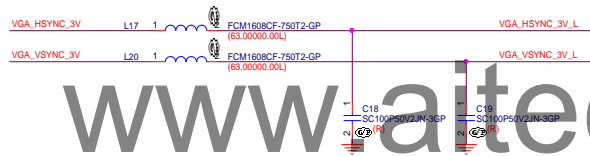
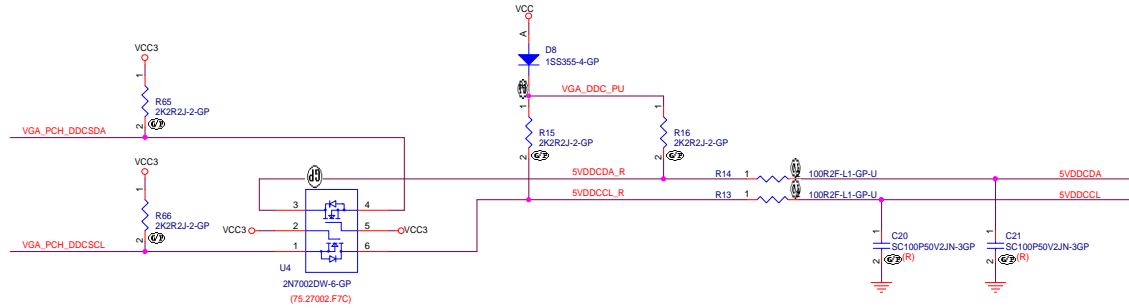
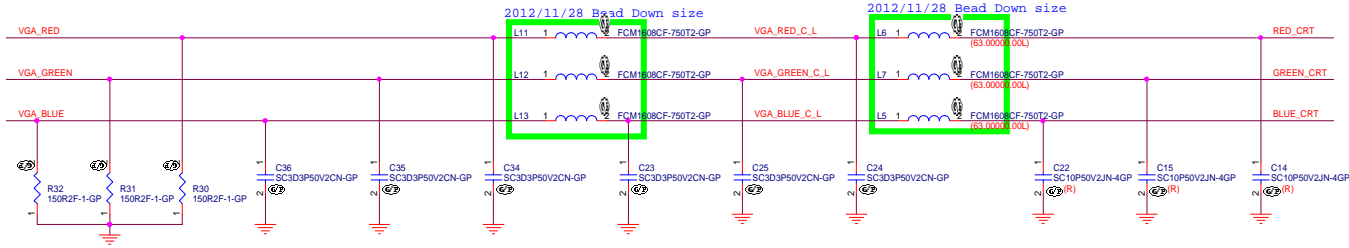
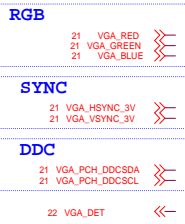
w/o Latch: 20.50352.164
with Latch: 20.50356.164

PCIE16 CONN may need LATCH if supporting 75W GFX Card

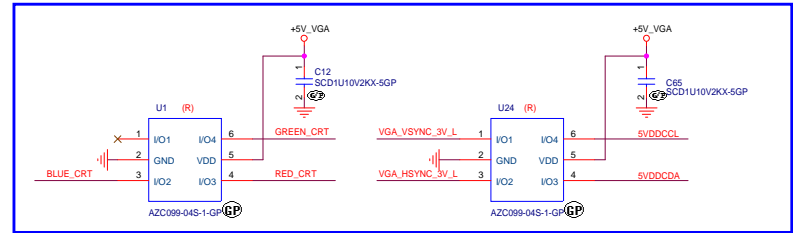
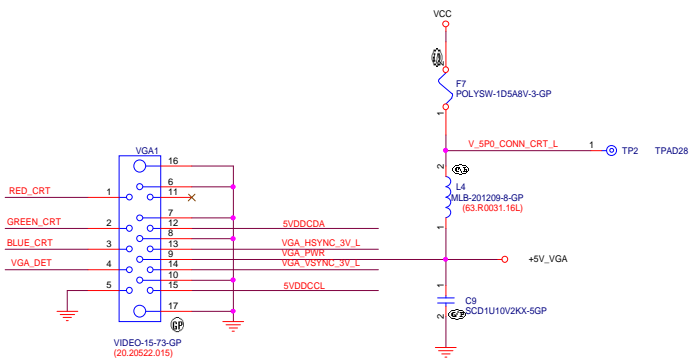


T-CONN164-4R4-GP
(20.50356.164)






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TBD

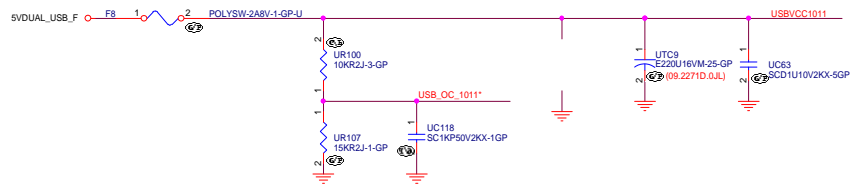
www.aitech1.ru

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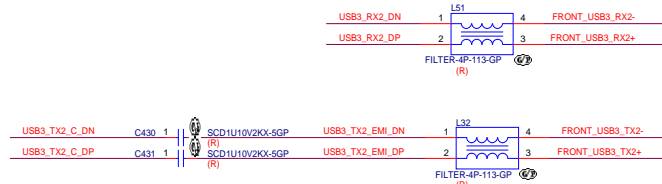
		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title TBD		
Size A	Document Number ROSA General-SFF	Rev -1A
Date: Thursday, August 15, 2013		Sheet 29 of 51

FRONT USB

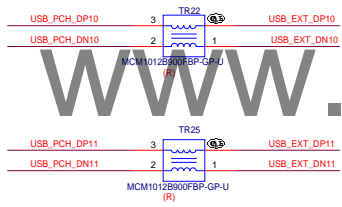
- 22 USB_PCH_DP10
- 22 USB_PCH_DN10
- 22 USB_PCH_DP11
- 22 USB_PCH_DN11
- 22 USB3_RX2_DN
- 22 USB3_RX2_DP
- 22 USB3_TX2_C_DN
- 22 USB3_TX2_C_DP
- 22 USB_OC_1011*
- 19 FB_USBF2_DET



USB 3.0



USB 2.0



ESD

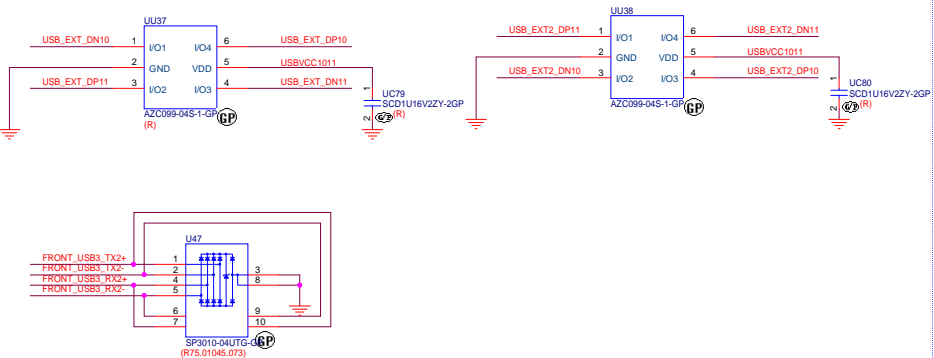
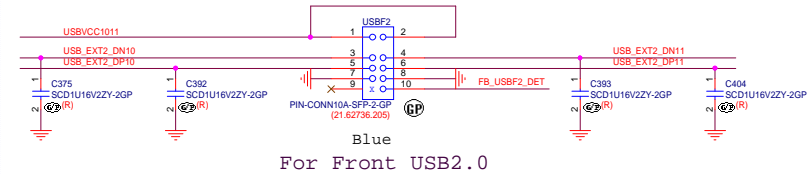
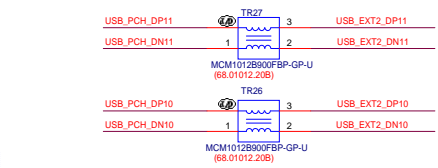
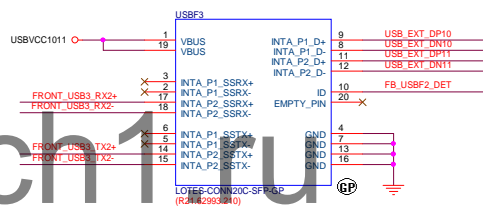


Table 2-1: USB3 ICC A Pin Assignment and Description

Pin No.	Signal	Description
1	Vbus	Power
2	IntA_P1_SSRX-	USB3 ICC Port1 SuperSpeed Rx-
3	IntA_P1_SSRX+	USB3 ICC Port1 SuperSpeed Rx+
4	GND	GND
5	IntA_P1_SSTX-	USB3 ICC Port1 SuperSpeed Tx-
6	IntA_P1_SSTX+	USB3 ICC Port1 SuperSpeed Tx+
7	GND	GND
8	IntA_P1_D-	USB3 ICC Port1 D- (USB2 Signal D-)
9	IntA_P1_D+	USB3 ICC Port1 D+ (USB2 Signal D+)
10	ID	Over Current Protection
11	IntA_P2_D+	USB3 ICC Port2 D+ (USB2 Signal D+)
12	IntA_P2_D-	USB3 ICC Port2 D- (USB2 Signal D-)
13	GND	GND
14	IntA_P2_SSTX+	USB3 ICC Port2 SuperSpeed Tx+
15	IntA_P2_SSTX-	USB3 ICC Port2 SuperSpeed Tx-
16	GND	GND
17	IntA_P2_SSRX+	USB3 ICC Port2 SuperSpeed Rx+
18	IntA_P2_SSRX-	USB3 ICC Port2 SuperSpeed Rx-
19	Vbus	Power




For Front USB2.0

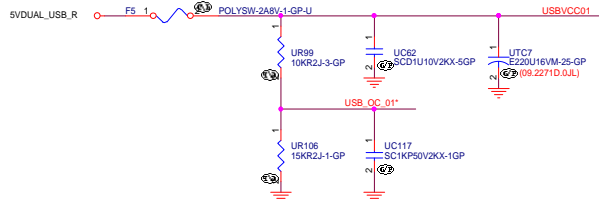
Title USB+RJ45				Rev
Size C	Document Number ROSA General-SFF			-1A
Date:	Thursday, August 15, 2013	Sheet	31	of 51

TBD

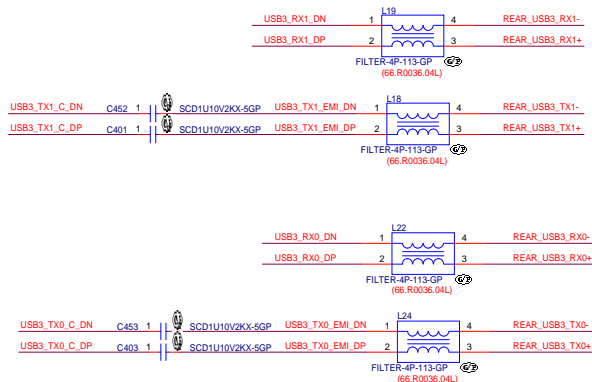
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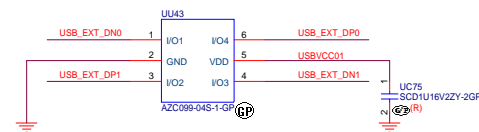
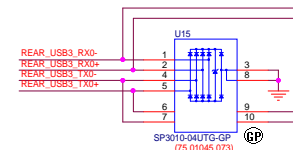
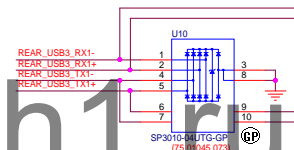
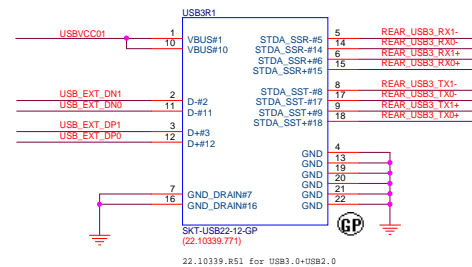
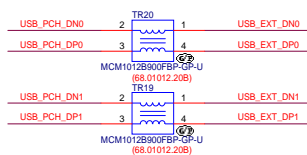
		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title TBD		
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USB 3.0



USB 2.0



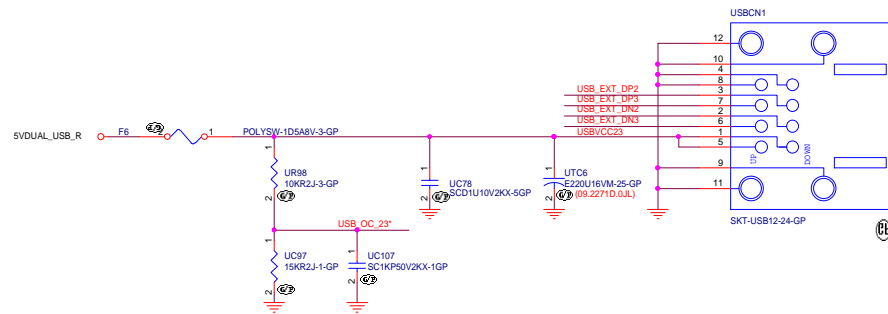
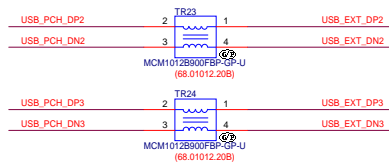
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Hsichih, Taipei

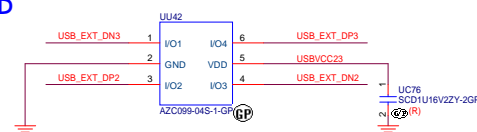
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REAR USB3.0			-1A
Size	Document Number		
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22 USB_PCH_DP2
22 USB_PCH_DN2
22 USB_PCH_DP3
22 USB_PCH_DN3
22 USB_PCH_DP4
22 USB_PCH_DN4
22 USB_OC_23*
22 USB_OC_45*
19 FB_USB1_DET

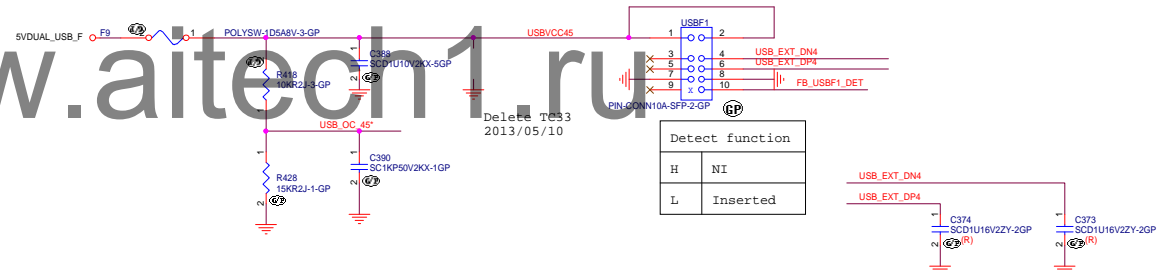
Rear USB 2.0



ESD

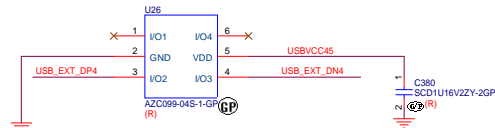


FRONT USB PORT

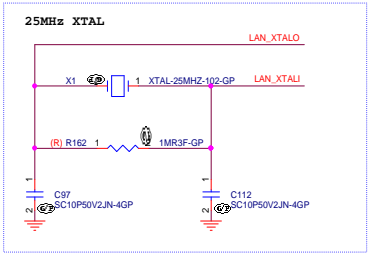
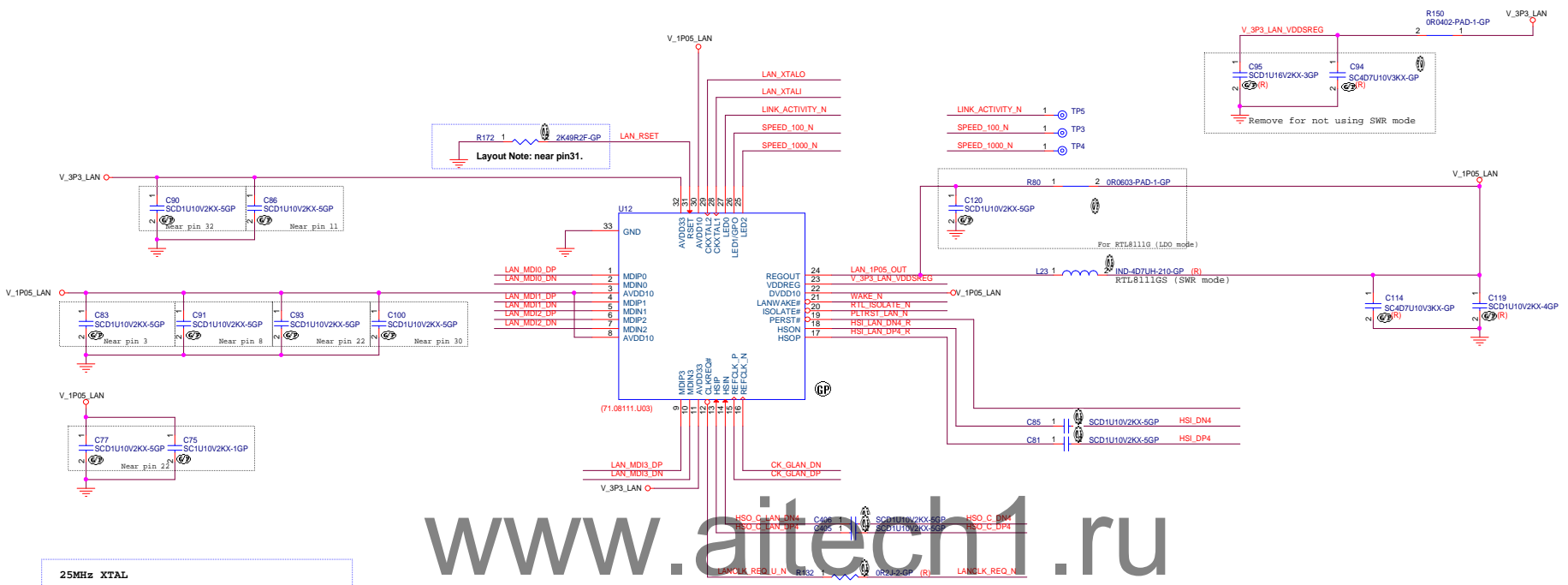


Detect function	
H	NI
L	Inserted

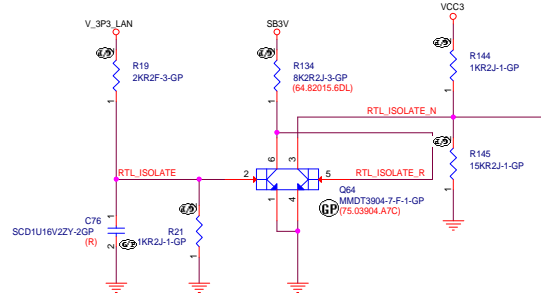
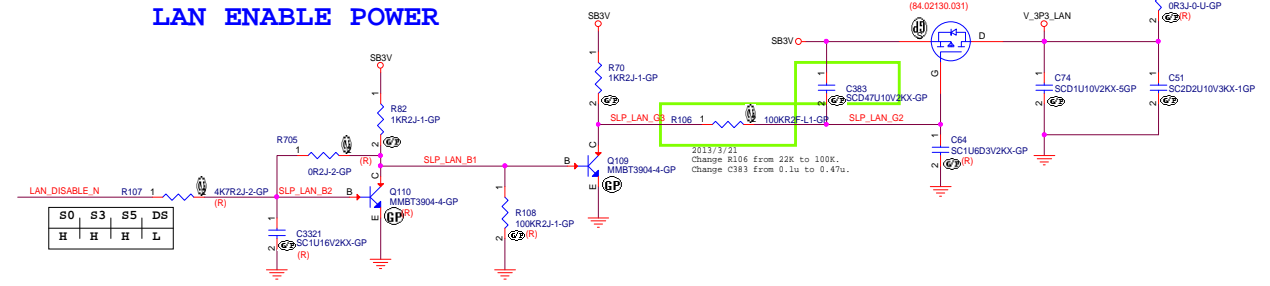
ESD

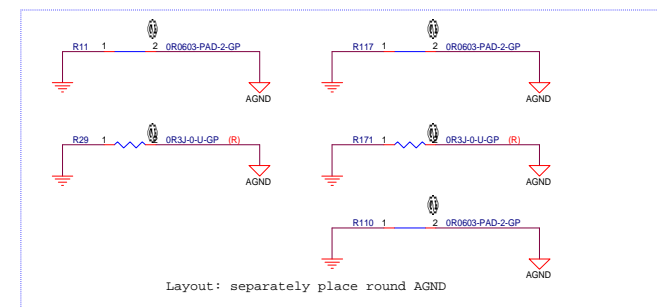
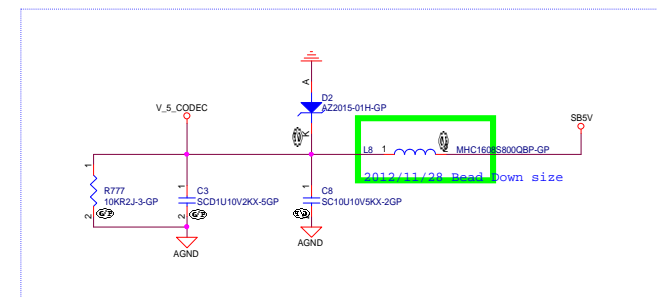
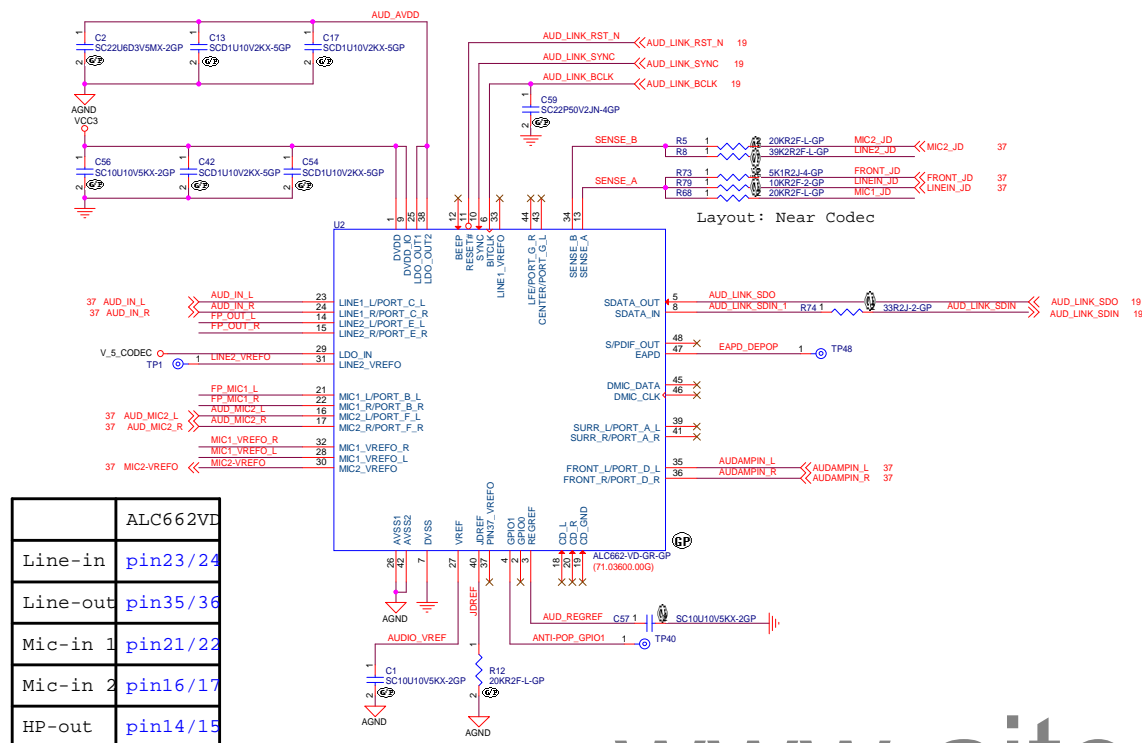


31 LAN_MDIO_DP
 31 LAN_MDIO_DN
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 31 LAN_MDIO_DN
 31 SPEED_100_N
 31 SPEED_1000_N
 31 LINK_ACTIVITY_N
 20 CK_GLAN_DP
 20 CK_GLAN_DN
 22 HSI_DN4
 22 HSI_DP4
 22 HSO_C_DN4
 22 HSO_C_DP4
 19 LANCLK_REQ_N
 39 PLTRST_LAN_N
 9,26,42,43 WAKE_N
 19 LAN_DISABLE_N



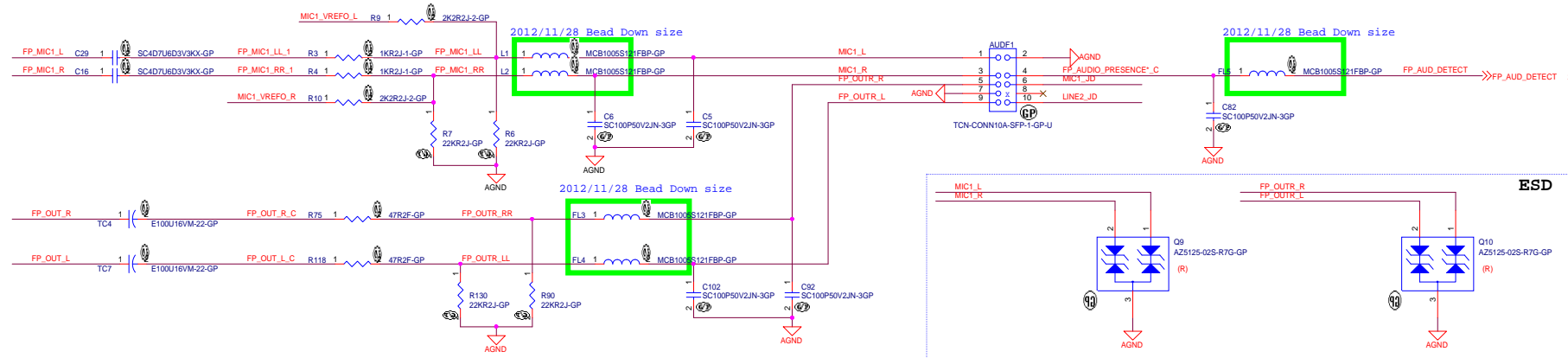
LAN ENABLE POWER

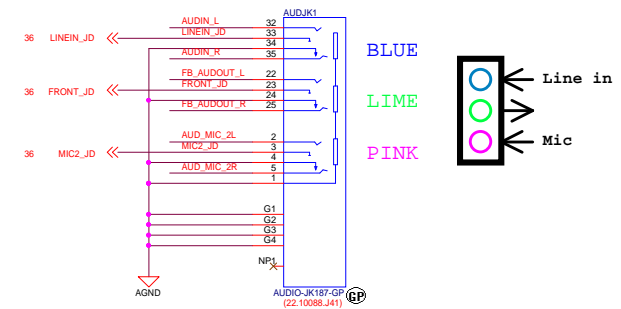
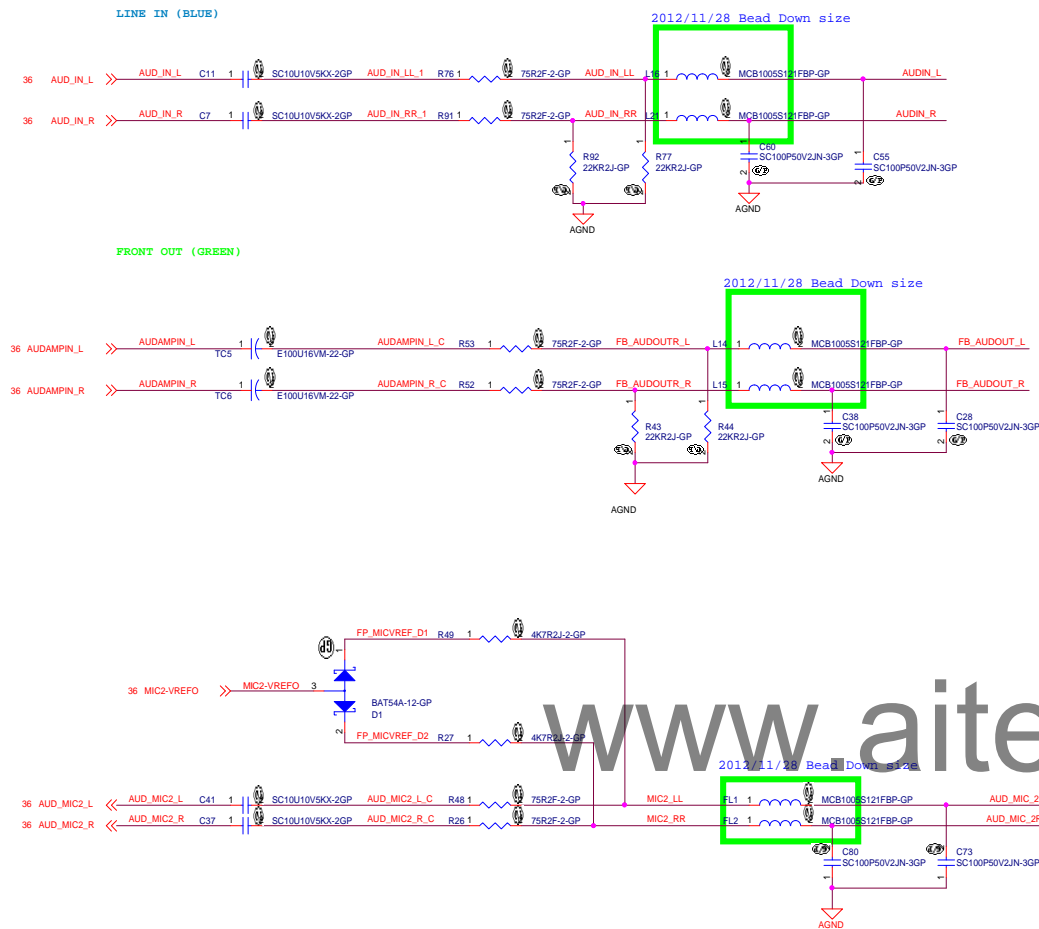




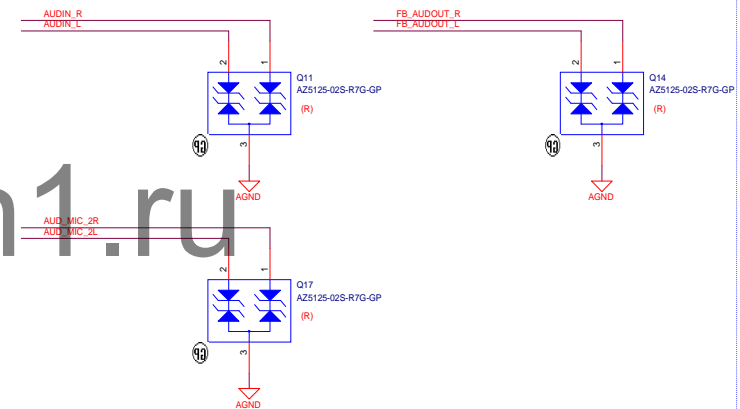
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Front Panel





ESD



<Variant Name>

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AUDIO JACKS

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ROSA General-SFF


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-1A

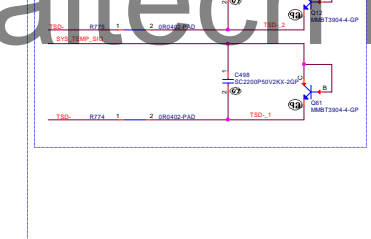
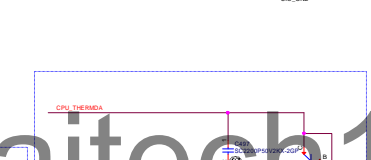
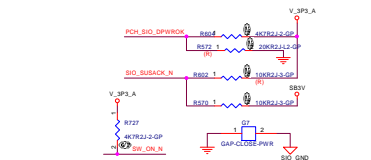
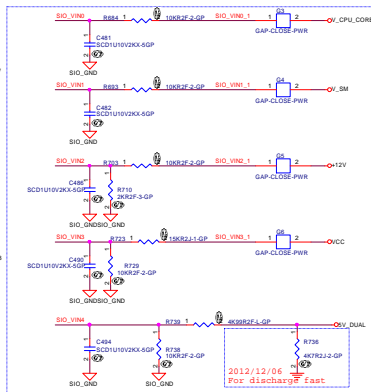
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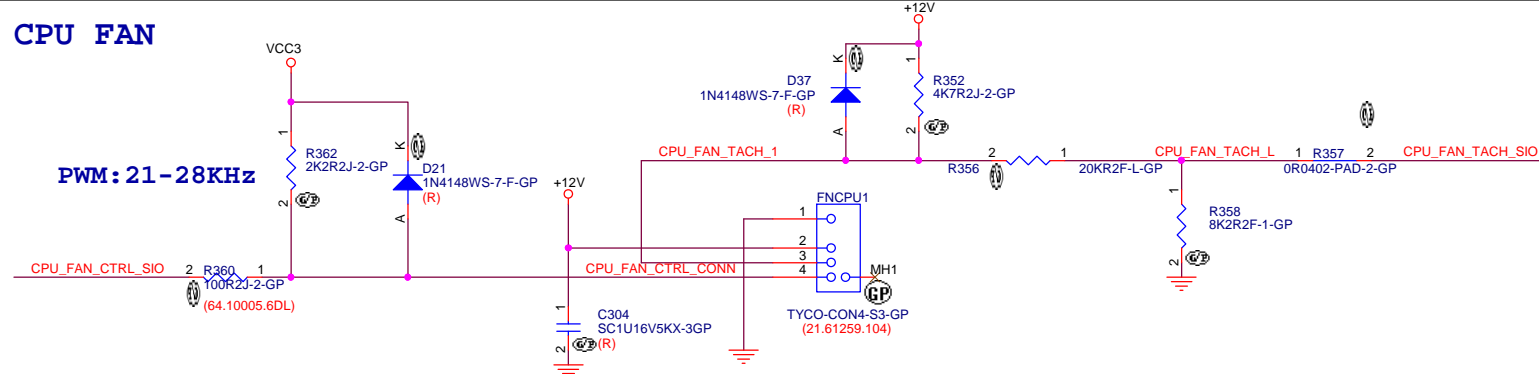
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		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title DSW			
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39 CPU_FAN_CTRL_SIO >>—
39 CPU_FAN_TACH_SIO <<—

PWM: 21-28KHz



2012/12/04 Ryan removed, ME Height filed

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Figure 1 shows the schematic diagram of the proposed 3-phase 3-wire 12-pulse rectifier circuit. The circuit is composed of three identical phase units connected in series. Each phase unit contains a 12-pulse diode bridge rectifier (represented by two 6-pulse bridges in series) and a 12-pulse transformer (represented by three 4-pulse transformers in series). The transformer windings are connected in a star configuration. The output of each phase unit is connected to a common neutral point (AGND). The input is a 3-phase 3-wire system with phases labeled H3, H4, and H5. The output is a 3-phase 3-wire system with phases labeled H2, H6, and H1. The transformer windings are labeled GENS315R158-8-F-A-G.

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1	Title
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FAN CIRCUITS/HOLE

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14,19,39 L_AD0

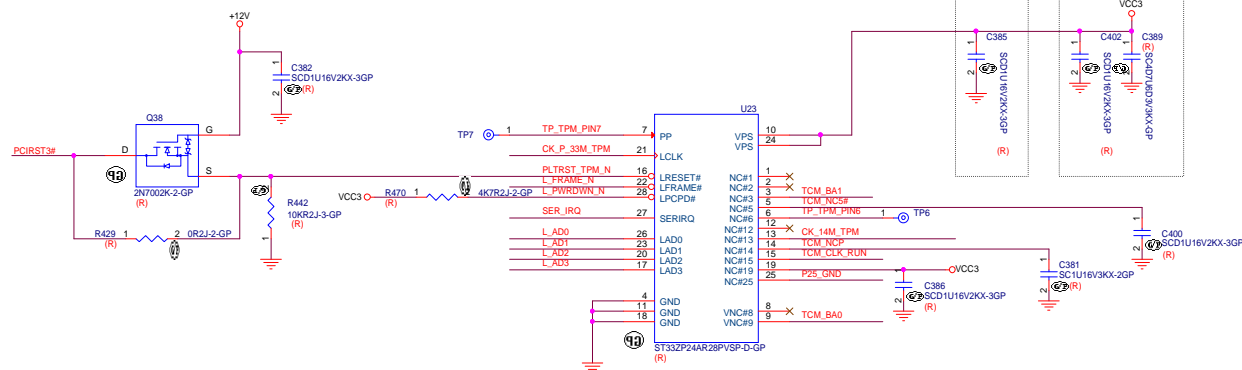
14,19,39 L_AD1

14,19,39 L_AD2

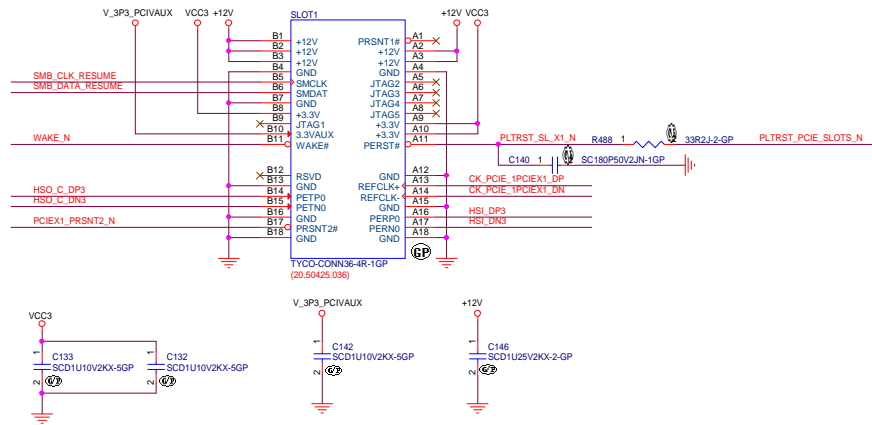
14,19,39 L_AD3

14,19,39 L_FRAME_N

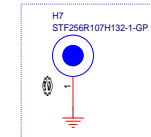
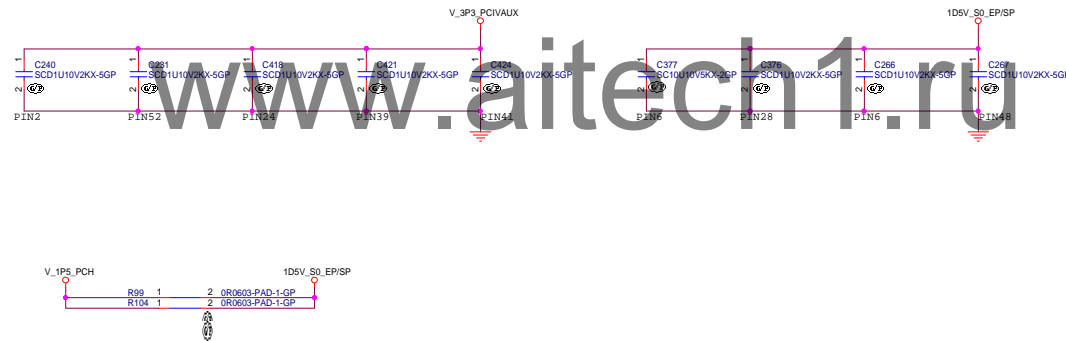
20 CK_P_33M_TPM >>—
21,39 SER_IRQ << >>—
14,39 PCIRST3# >>—
20 CK_14M_TPM >>—



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Title

EMC

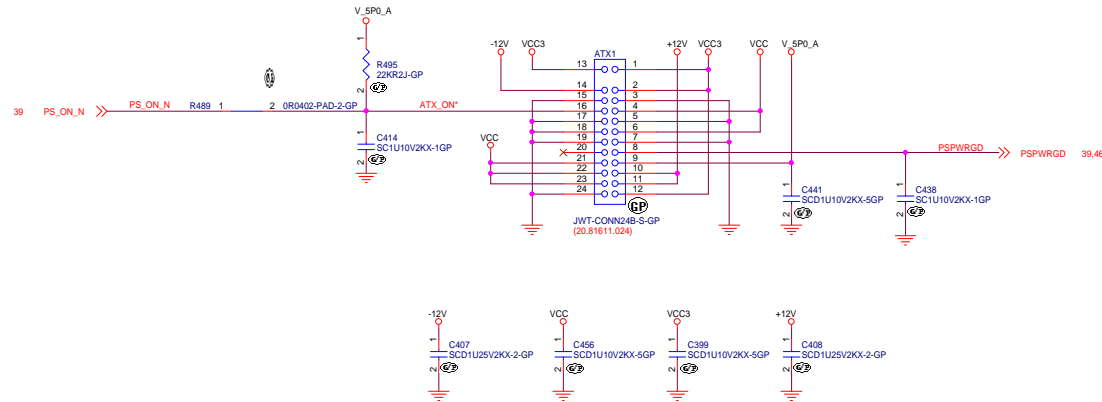
Size
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Document Number
ROSA General-SFF

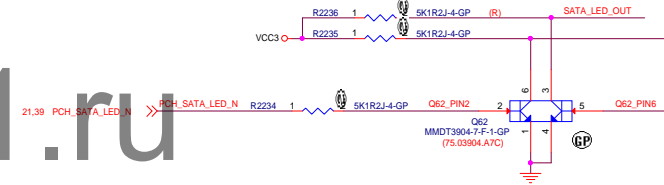
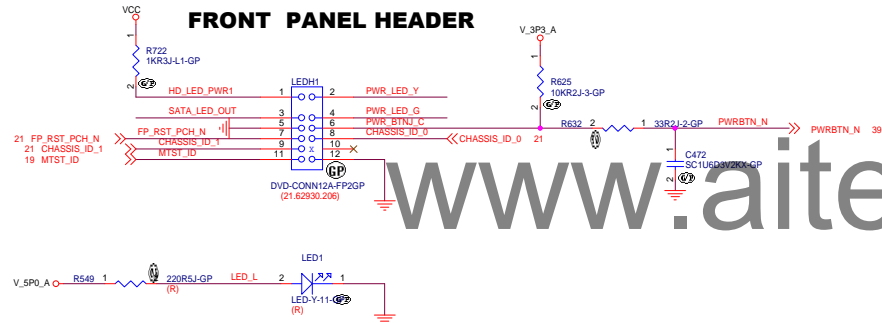
Rev
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ATX CONNECTOR

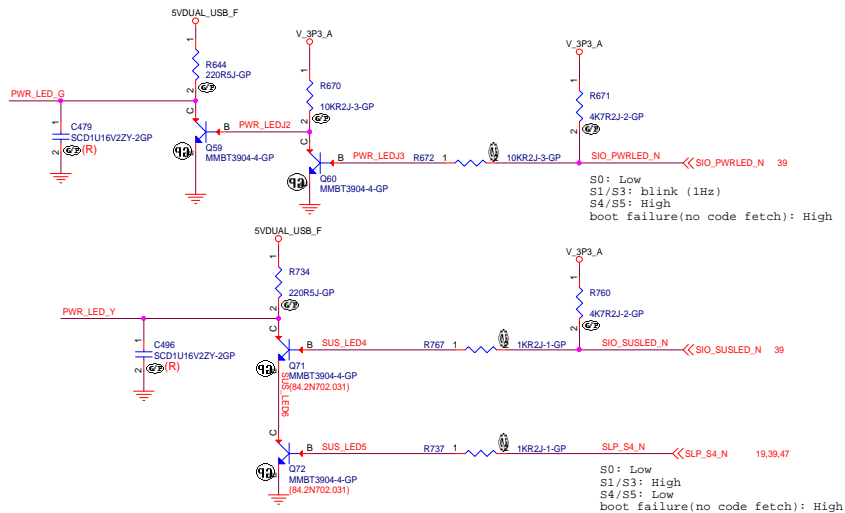


FRONT PANEL HEADER




White LED Amber LED

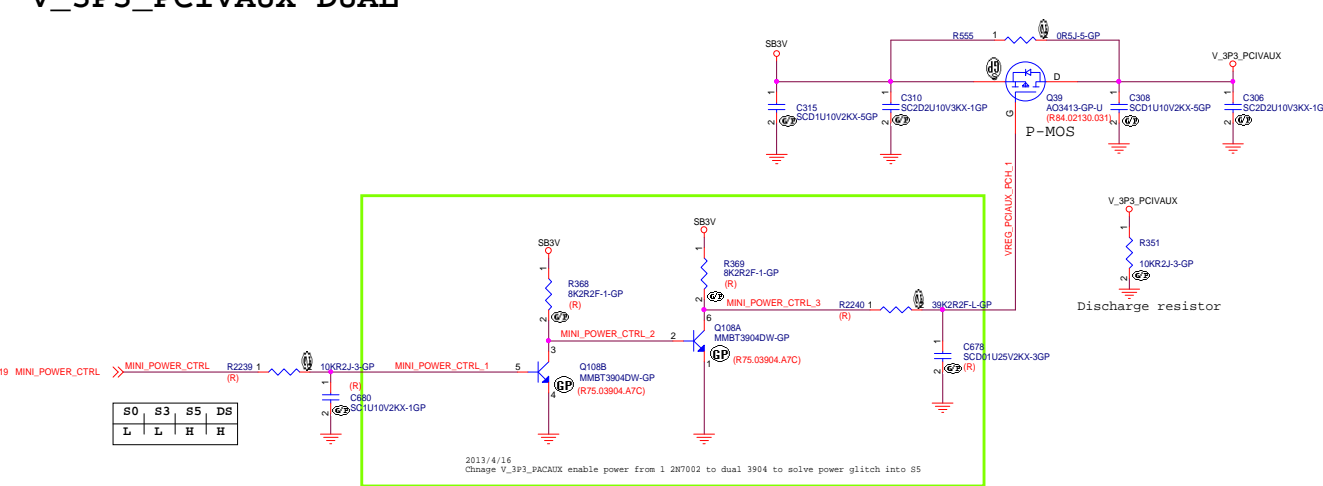
S0	White
S3	Amber
S4	LED off
No Post	Amber
Failure to Post	Amber (blinking)



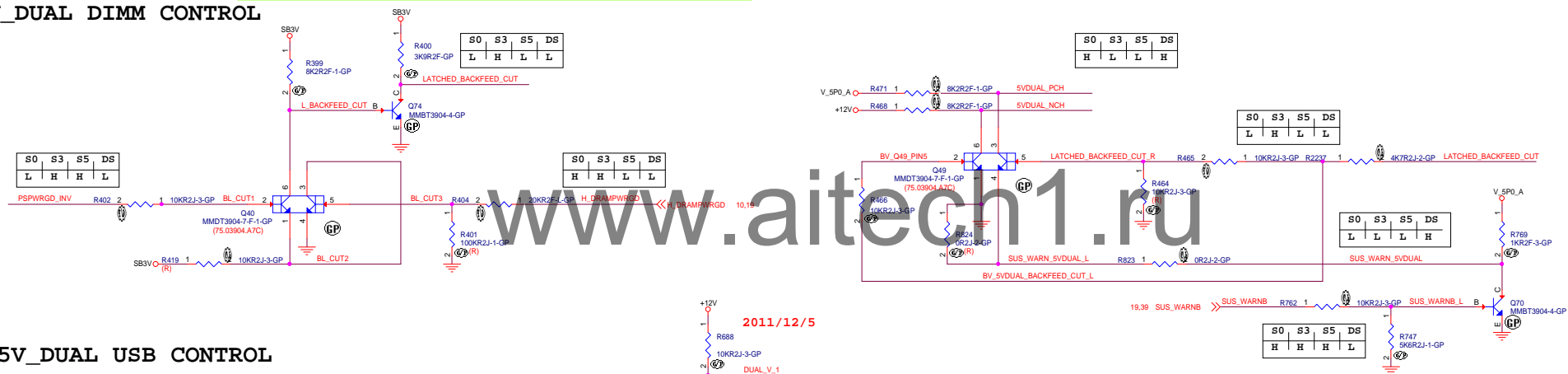
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Title PWR/FNT PNL			
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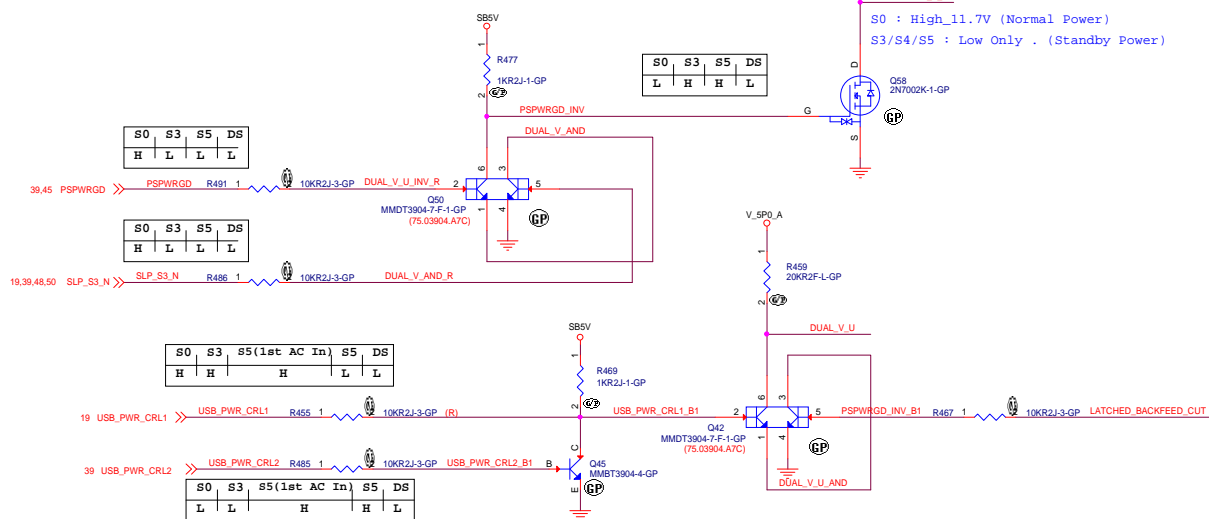
V_3P3_PCIV AUX DUAL



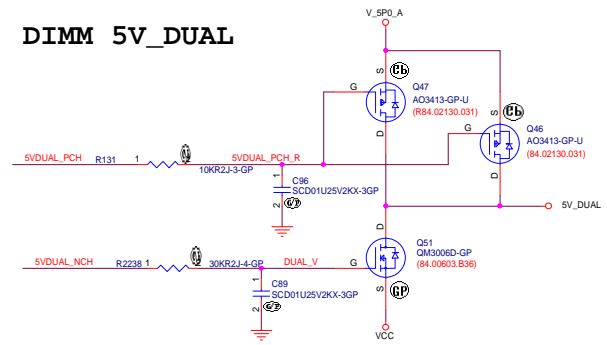
5V_DUAL DIMM CONTROL



5V_DUAL USB CONTROL



DIMM 5V_DUAL



	S0	S3	S5	I
5V_DUAL	VCC	V_5P0_A	V_5P0_A	0

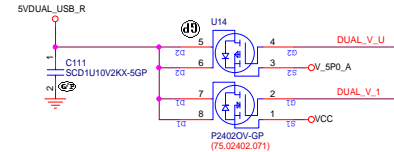
S0	S3	S5	D
H	L	L	H

S0	S3	S5	DS
L	H	L	L

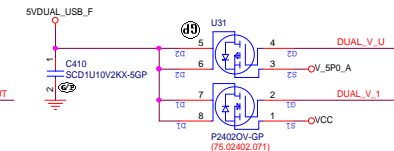
S0	S3	S5	DS
L	L	L	H

S0	S3	S5	DS
H	H	H	L

REAR PORT



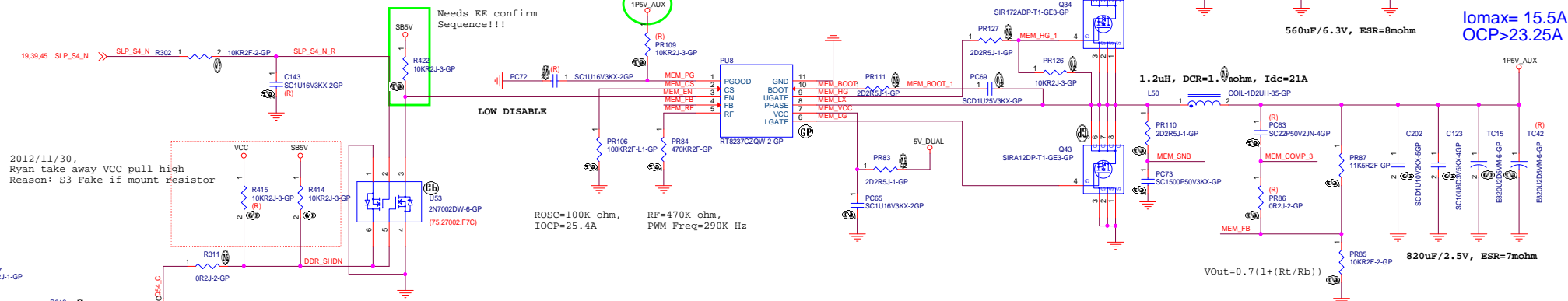
FRONT PORT



	S0	S3	S5	DS
5VDUAL_USB_R	VCC	SB5V	0	0
5VDUAL_USB_F	VCC	SB5V	0	0

S0	S3	S5	DS
H	H	L	L


84.00172.A37 SIR172ADP 84.SRA12.037 SIRAI2DIP
Vgs @ 4.5V, Vgs @ 4.5V,
Id = 12.9A, Id = 20A,
Rds(on) = 8.5-10.5mohm, Rds(on) = 4.4-6.0mohm,



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Title ME POWER			
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SharkBay VR12.5 POWER CKT - 3 PHASE

